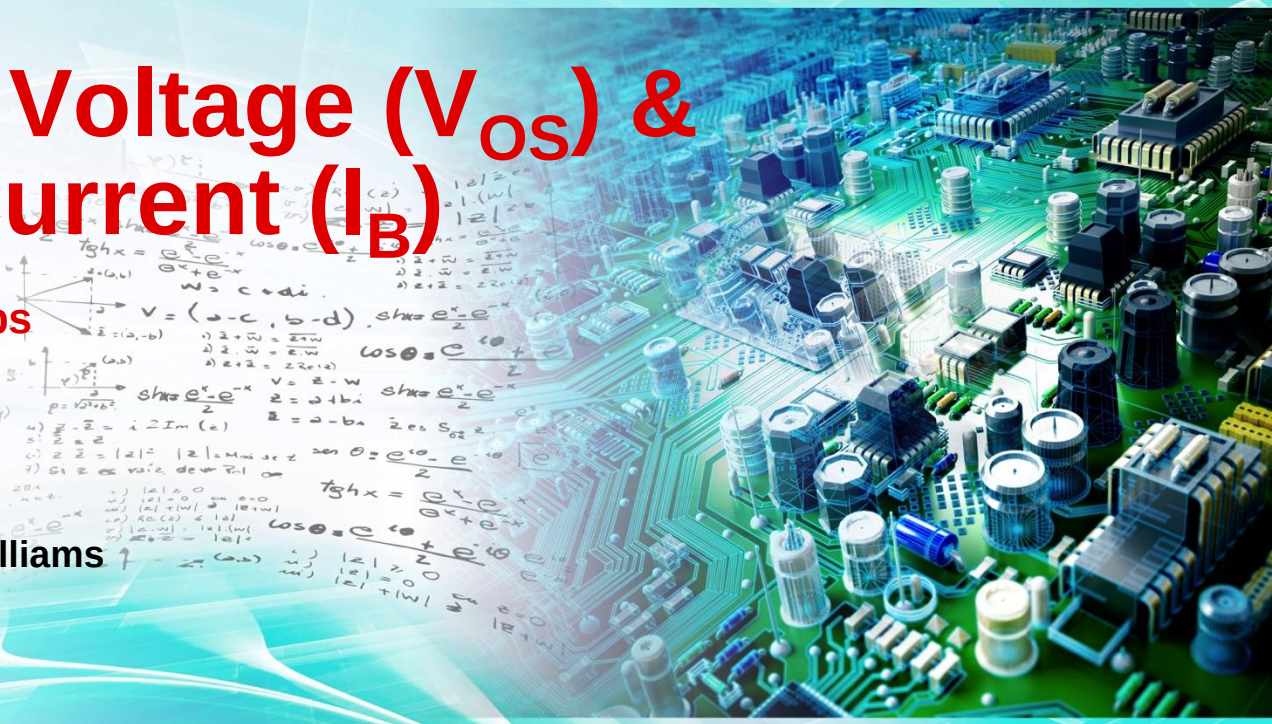
Input Offset Voltage (V_{OS}) & Input Bias Current (I_B)

TIPL 1100
TI Precision Labs – Op Amps



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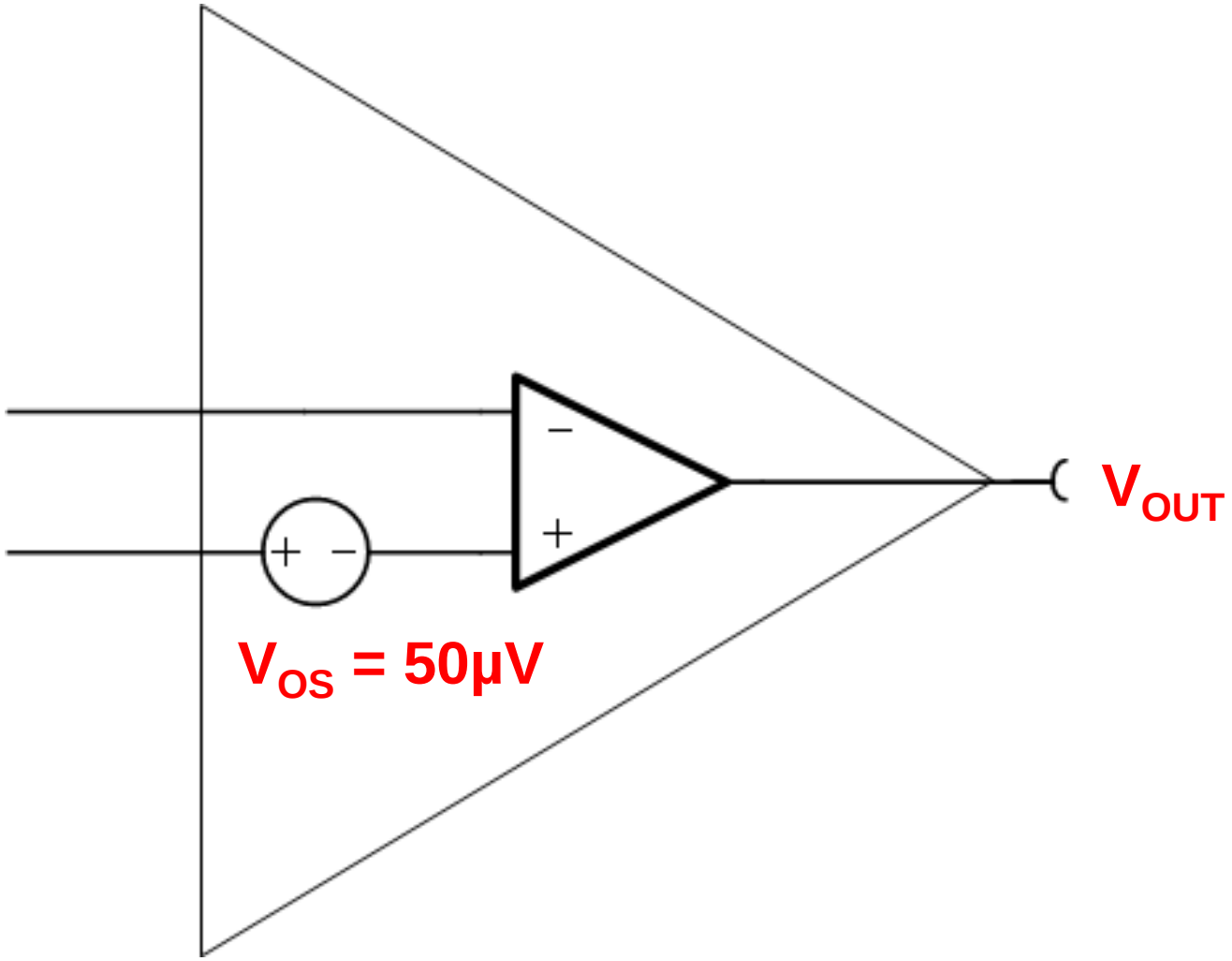
Prepared by Art Kay and Ian Williams

Hello, and welcome to the TI Precision Lab discussing input offset voltage, VOS, and input bias current, IB. In this video we'll discuss op amp V_{OS} specifications, V_{OS} drift over temperature, input bias current specifications, and input bias current drift over temperature. We'll also show the range of V_{OS} and I_B across many different Texas Instruments op amps.

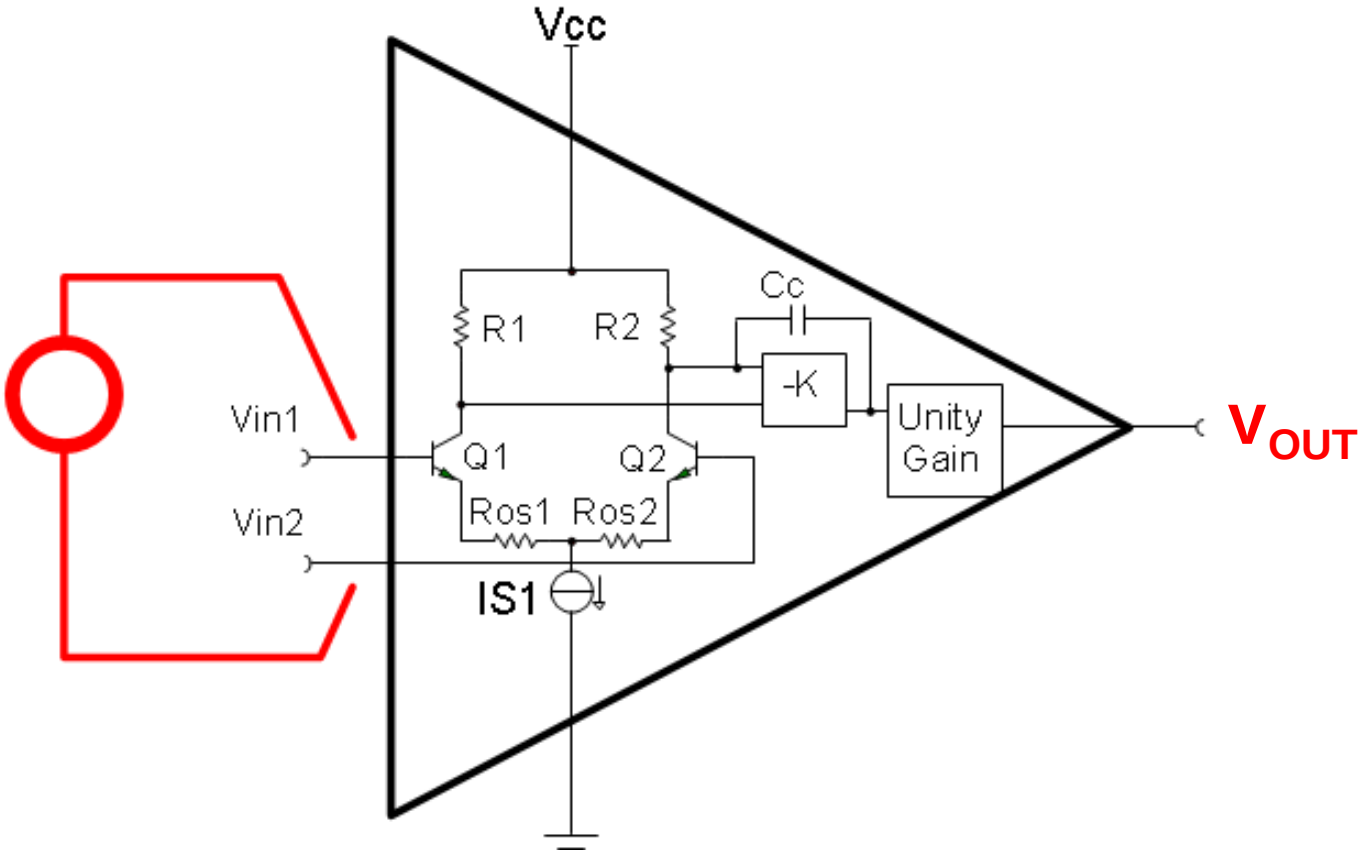
Input Offset Voltage - V_{OS}



Let’s start by defining offset voltage. Offset voltage is the differential input voltage that would have to be applied to force the op amp’s output to zero volts. Typical offset voltages range from mV down to µV, depending on the op amp model. Offset can be modeled as an internal dc source connected to the input of the op amp. Changing power supply voltage and common mode voltage will affect input offset voltage.

Input Offset Voltage - V_{OS}

Input offset from mismatch of input transistors



Looking at the inside of an op amp, we can see that the mismatch of transistors Q_1 and Q_2 in the differential input pair is what causes the offset voltage. In some cases, internal resistors R_{OS1} and R_{OS2} are laser trimmed in order to compensate for this mismatch and obtain very low offset voltage. In other cases, an internal digital correction circuit is used to minimize offset voltage and offset drift.

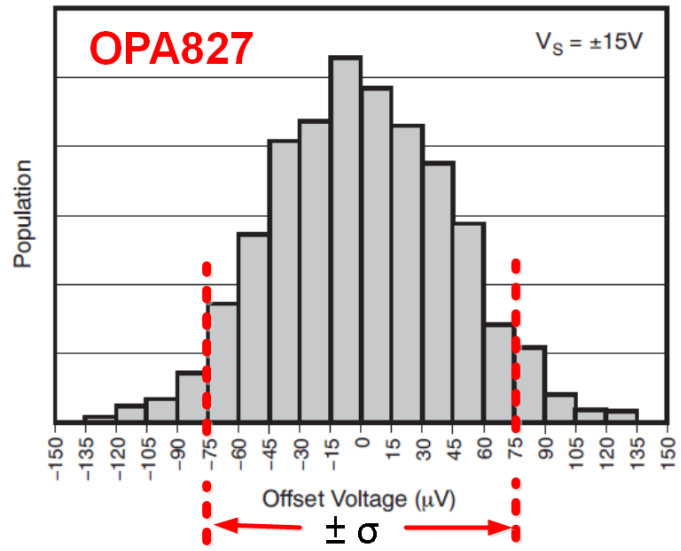
Offset Voltage Specs and Distribution

ELECTRICAL CHARACTERISTICS: V_S = ±4V to ±18V

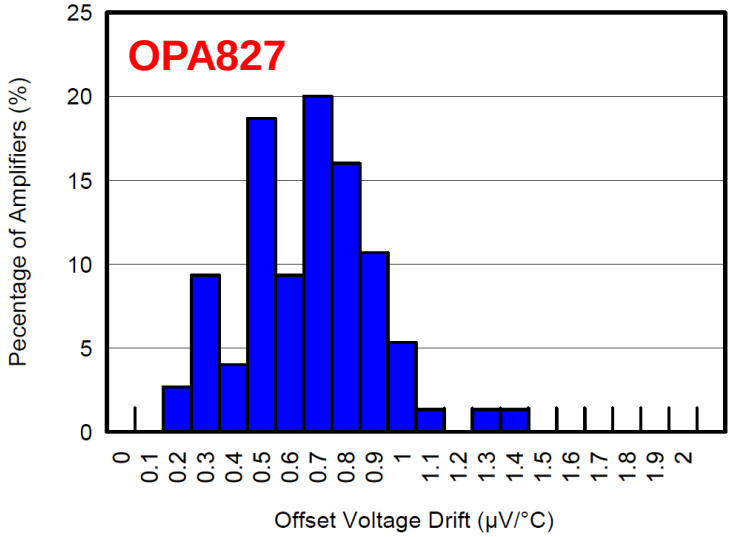
Boldface limits apply over the specified temperature range, T_A = –40°C to +125°C.
At T_A = +25°C, R_L = 10kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		CONDITIONS	OPA827AI			UNIT
			MIN	TYP	MAX	
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = ±15V, V_{CM} = 0V		75	150	µV
Drift	**dV_{OS}/dT**			**0.1**	**2.0**	**µV/°C**
vs Power Supply	PSRR			0.2	1	µV/V
Over Temperature					**3**	**µV/V**

OFFSET VOLTAGE PRODUCTION DISTRIBUTION



OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



This slide introduces op amp specifications. The top of the specification table is the test conditions for all the parameters in the data sheet. In this example, the temperature is 25 °C, the load resistance is 10k Ω, the load is connected to mid supply, and the common mode voltage is set to mid supply. These conditions are true unless otherwise specified. If you look at the offset voltage specs, it lists some additional conditions. The supply voltage is +/-15V and the common mode voltage is 0V.

Note that we also have standard grade and a high grade for this part. Not all devices will have a high grade. The high grade device will have better performance than the standard grade device for some key specifications. In this case, the high grade device has a lower input offset voltage. Also note that we have a typical and a maximum specification. The value listed in the typical specification will cover ± one standard deviation, or ± sigma, on a Gaussian distribution. This means that 68% of the device population will be less then the typical value. So, in this example, 68% of the devices would have less then ±75 µV of V_{OS}. The maximum is a tested value, and so you will never find a device with greater than the maximum V_{OS} of ±150 µV .

We also have a V_{OS} drift specification that is measured in µV/°C, describing how V_{OS} changes with temperature. In this case, the typical drift is given as 0.1 µV/°C. The maximum drift is given as 2 µV/°C.

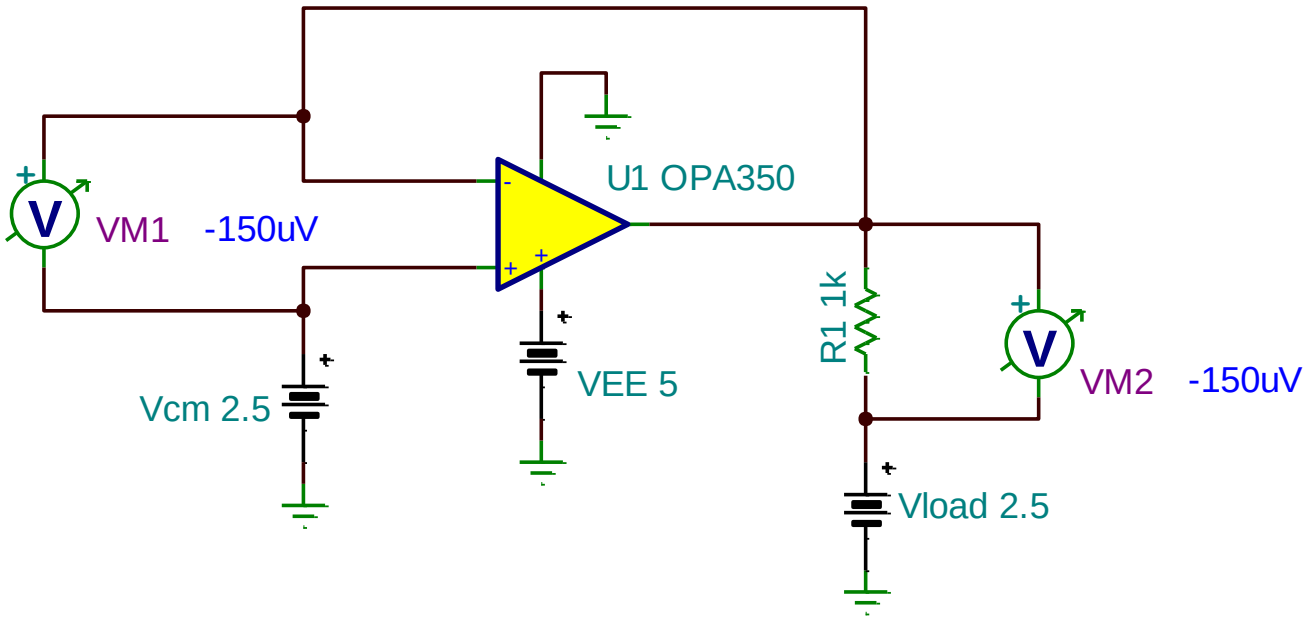
Simulate Input Offset Voltage

ELECTRICAL CHARACTERISTICS: V_S = 2.7V to 5.5V

Boldface limits apply over the temperature range, **T_A = −40°C to +85°C**. V_S = 5V.

All specifications at T_A = +25°C, R_L = 1kΩ connected to V_S/2 and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA350, OPA2350, OPA4350 MIN	TYP(1)	MAX	UNIT
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = 5V		±150	±500	µV
T_A = −40°C to +85°C					±1	mV

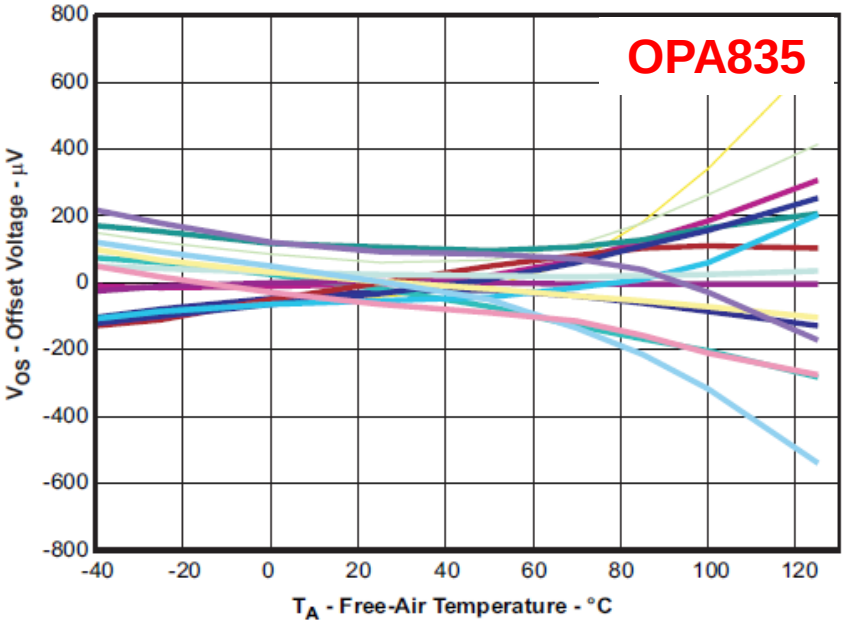


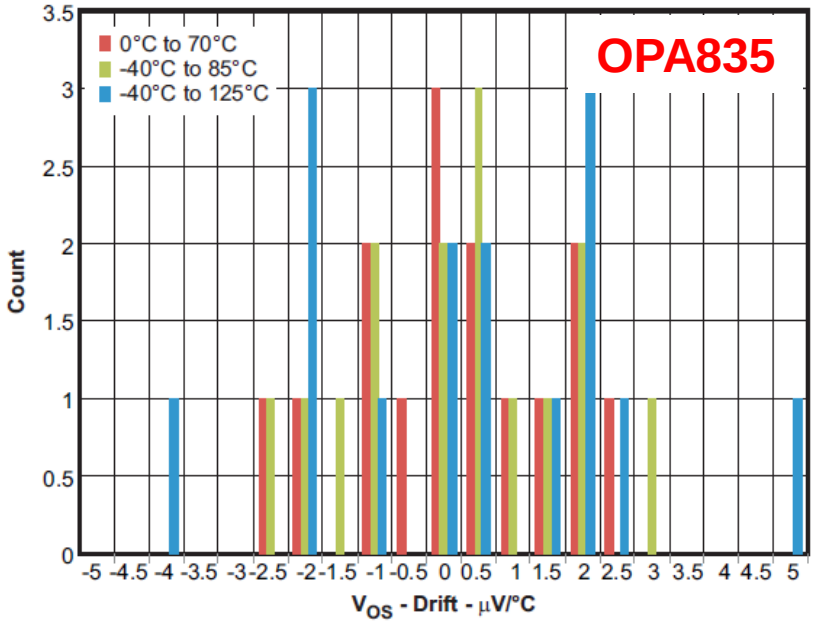
01 - Vos - OPA350.TSC

Most op amp SPICE models include the effects of offset voltage. Several external conditions, such as power supply voltage and common mode voltage, affect the offset voltage on a real world device. These effects are also included in the simulation model.

In order for the simulation result to match the offset specifications in the data sheet table, the same test conditions must to be applied to the amplifier. In this example, the power supply is set to 5 V, the common mode voltage is set to mid supply, or 2.5 V, and the load is connected to mid supply in order to match the data sheet conditions. The typical offset specification is 150 µV, and the simulated offset is also 150 µV. The goal of our models is to target typical op amp performance.

Drift Slope – Positive and Negative



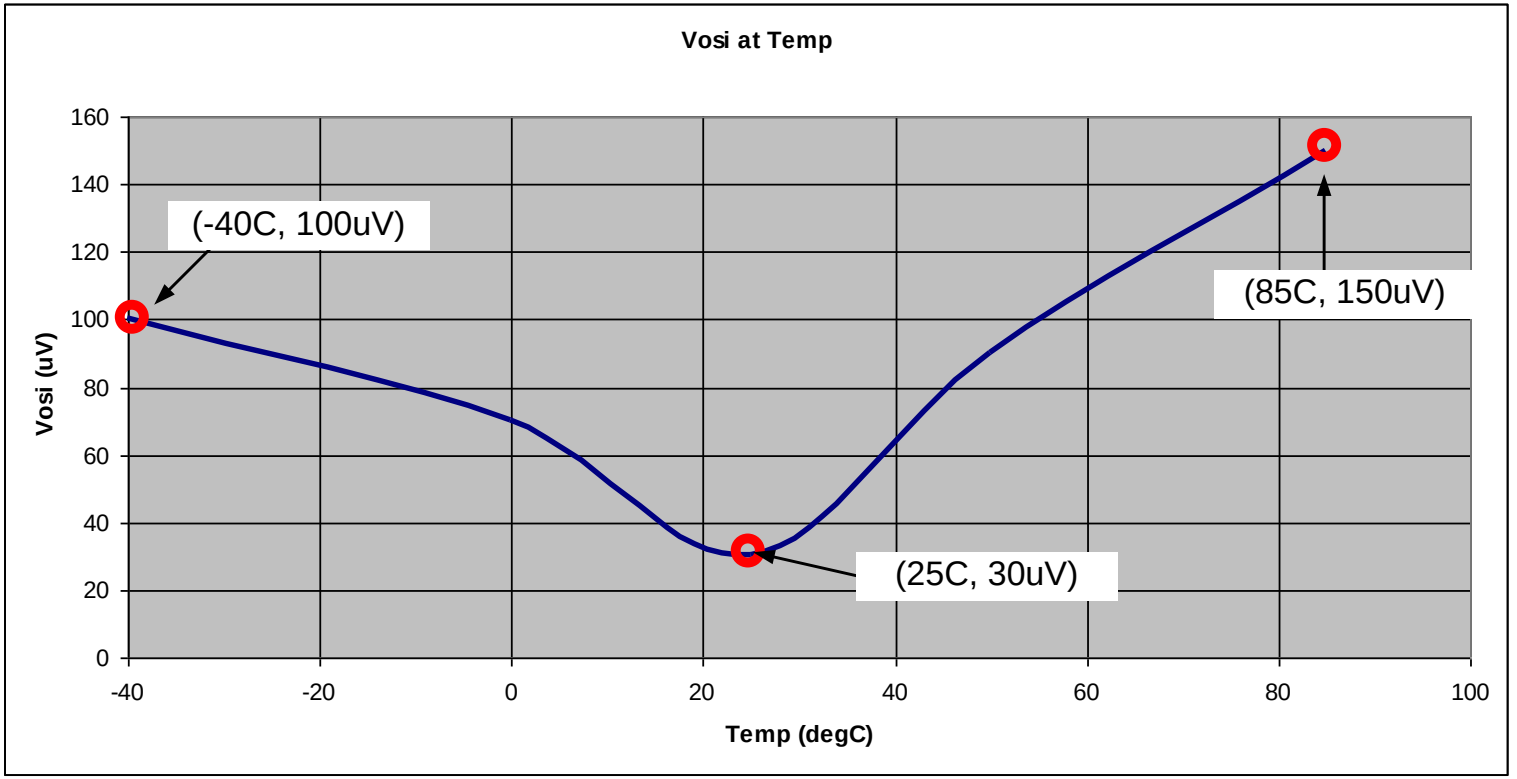


For this example V_{OS} drift is defined as:

$$\frac{\Delta V_{os}}{\Delta T} = \frac{V_{os}(T_1) - V_{os}(25C)}{T_1 - 25C}$$

The slope on offset voltage drift can be either positive or negative. This formula shows one possible definition for offset drift. This formula will produce a positive or negative drift depending on the slope of the curve. Some other definitions use the absolute value, so you will not have a negative offset.

Drift Slope – Common Definition



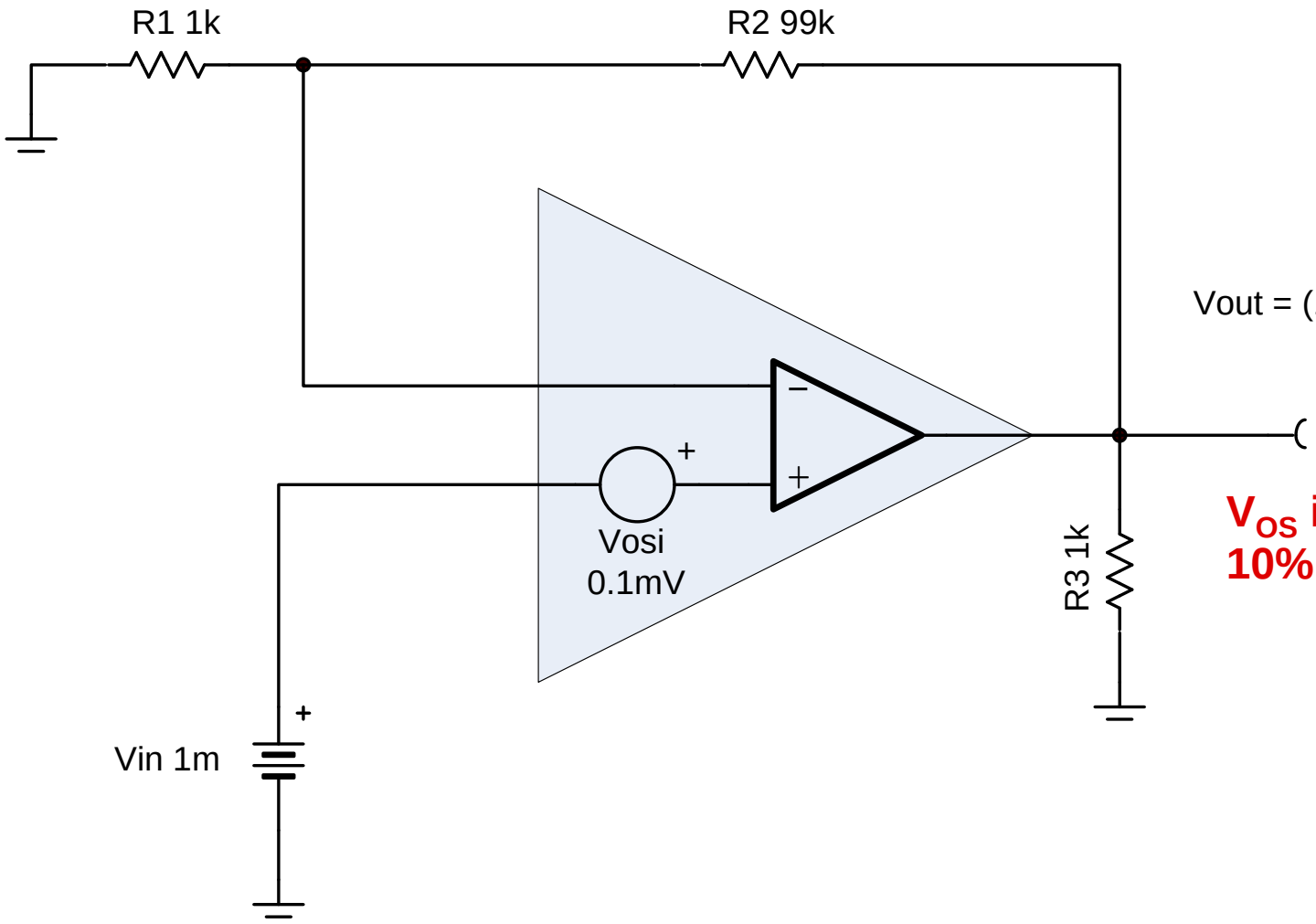
$$\frac{\Delta V_{os}}{\Delta T} = \frac{\left|V_{os}(T_1) - V_{os}(25C)\right| + \left|V_{os}(T_2) - V_{os}(25C)\right|}{\left|T_1 - T_2\right|}$$

$$\frac{\Delta V_{os}}{\Delta T} = \frac{\left|100\mu V - 30\mu V\right| + \left|150\mu V - 30\mu V\right|}{\left|85C - (-40C)\right|} = 1.52\,\frac{\mu V}{^{\circ}C}$$

This is the more common definition for drift, which is separated into different two regions, although more than two regions could be used if desired.

The idea with this definition is that you get a more realistic view of what the expected error would be than if you only considered the end points over the entire region. In this example, you can see that the slope of the two separate regions is much more severe than the drift of the entire range. Note that the absolute value is used in the formula, so this formula will never give a negative result.

Application Example

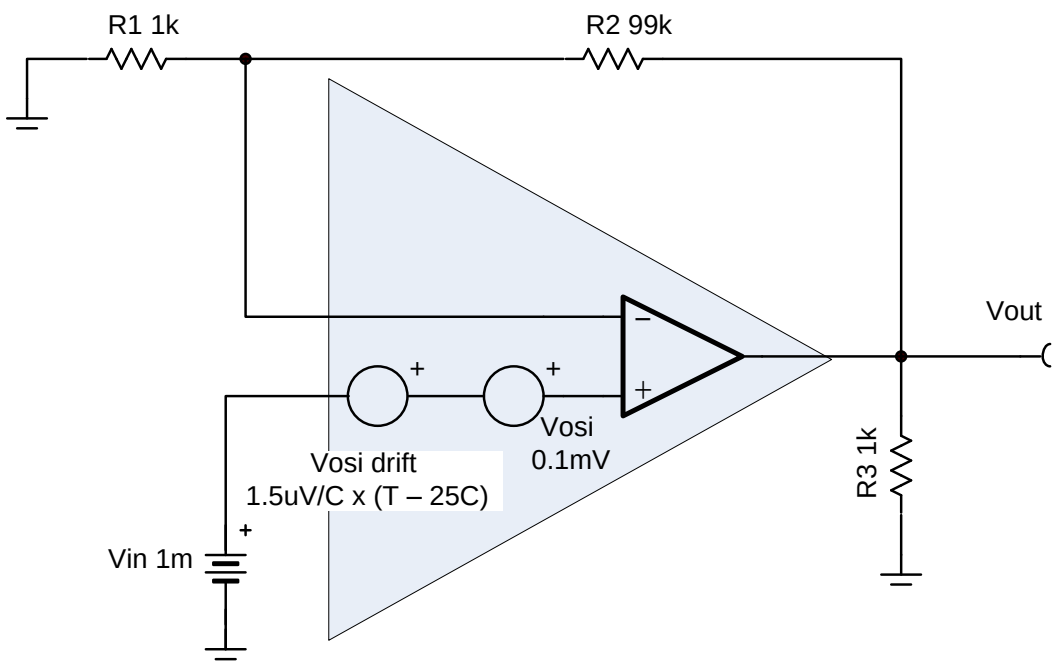


In this application example we will see how to calculate the output voltage error from the offset voltage.

Consider offset voltage as a dc voltage source in series with the non-inverting input of the op amp. We have a 0.1mV or 100uV offset in this case. The signal source is a very small input of 1mV, so the offset will generate a fairly significant error. The gain for this part is configured as 100 V/V, which can be calculated as R2/R1 + 1.

The total output voltage is the series combination of the offset and the input signal (1mV + 0.1mV), multiplied by the gain (100), which gives us 110 mV. The offset accounts for about 10% error.

Input Offset Drift Calculations



Temp (°C)	V_{os} Initial + Drift +1.5uV/C	V_{os} Initial + Drift -1.5uV/C
-25 °C	25uV	175uV
0 °C	62.5uV	137.5uV
25 °C	100uV	100uV
50 °C	137.5uV	62.5uV
85 °C	190uV	10uV
125 °C	250uV	-50uV

$$V_{osi} = V_{osi\_room} + V_{osi\_drift} \cdot (T - 25C)$$

Example calculations:

$$V_{osi} = 100\mu V + 1.5\frac{\mu V}{C} \cdot [(25C) - 25C] = 100\mu V \qquad \text{At 25C}$$

$$V_{osi} = 100\mu V + 1.5\frac{\mu V}{C} \cdot [(125C) - 25C] = 250\mu V \qquad \text{At 125C}$$

Offset drift calculations can be done in a similar manner. Notice that we have two sources: one for the initial offset and one for the offset drift. The offset drift source will be zero at 25C. As the temperature deviates from 25C, the temperature difference will be multiplied by the offset drift to generate the additional offset voltage.

For example, at 25C we have 100uV of offset, which is just the room temperature offset and no drift term. At 125C we have a total of 250uV; that is, 100uV from the initial offset, and 150uV from the drift term.

The table on the right illustrates how the offset changes over temperature. Keep in mind that the slope of the offset drift can be either positive or negative, so both cases are shown.

Drift is especially important in calibrated systems. In calibrated systems, room temperature offset is frequently measured and corrected for in software. Temperature drift, however, is often difficult and expensive to calibrate out, so devices with minimal drift are preferable.

Range of Offset - µV to mV

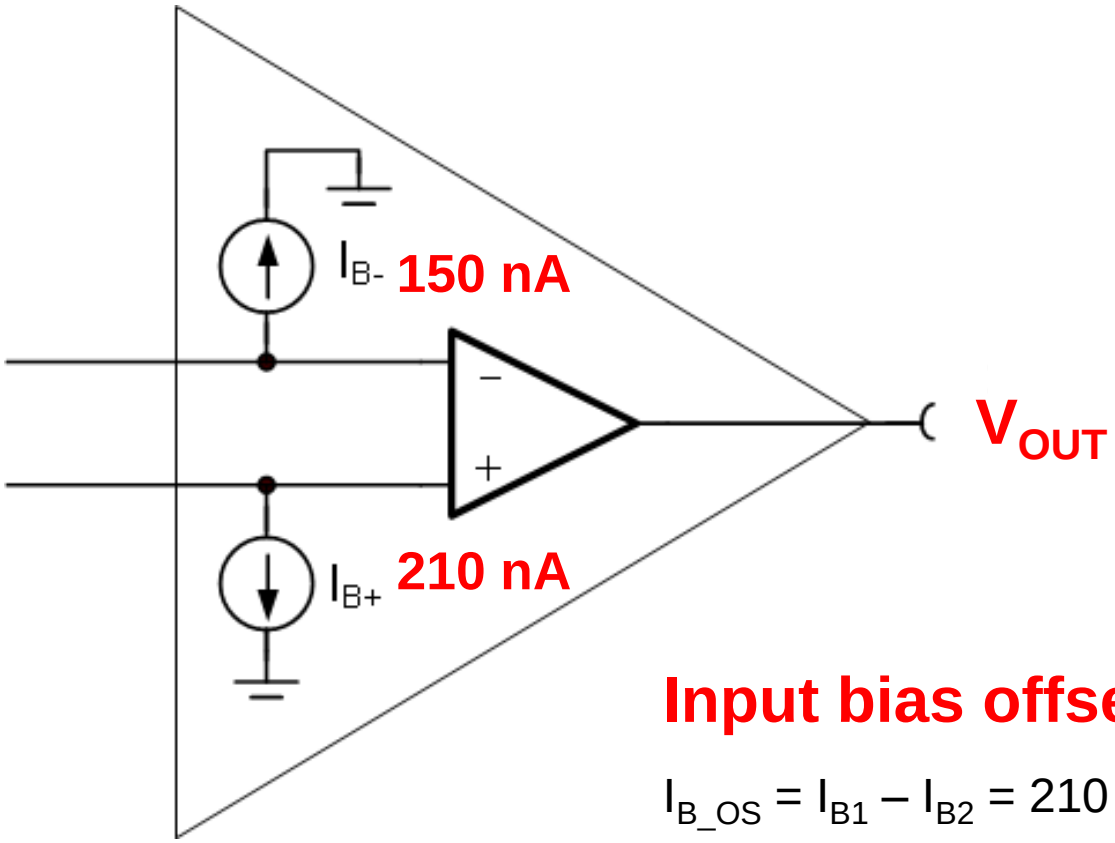
Op Amp	V_{OS} (max) (high grade)	V_{OS} Drift (max) (high grade)	Technology
OPA333	10 µV	0.05 µV/°C	Zero Drift CMOS
OPA277	20 µV	0.15 µV/°C	Precision Bipolar
OPA188	25 µV	0.085 µV/°C	Auto-Zero CMOS
OPA192	25 µV	0.5 µV/°C	CMOS
OPA211	50 µV	1.5 µV/°C	Precision Bipolar
OPA827	150 µV	1.5 µV/°C (typ.)	JFET input, Bipolar, Precision
OPA350	500 µV	4 µV/°C (typ.)	CMOS
OPA835	1.85 mV	13.5 µV/°C	High Speed Bipolar
LM741	3.00 mV	15 µV/°C	Bipolar commodity (lower cost)

This chart shows a range of offset voltages, from uV to mV, for different types of TI amplifiers.

The first amplifier in the list, the OPA333, includes a zero drift topology which uses an internal digital calibration circuit to minimize offset and offset drift. Some precision bipolar amplifiers use laser trimming to minimize offset.

Often you must trade off bandwidth or other characteristics for low offset. For example, the OPA835 is optimized for speed, not for offset. Also, commodity, or low cost amplifiers are usually not optimized for low offset or offset drift.

Input Bias Current - I_B



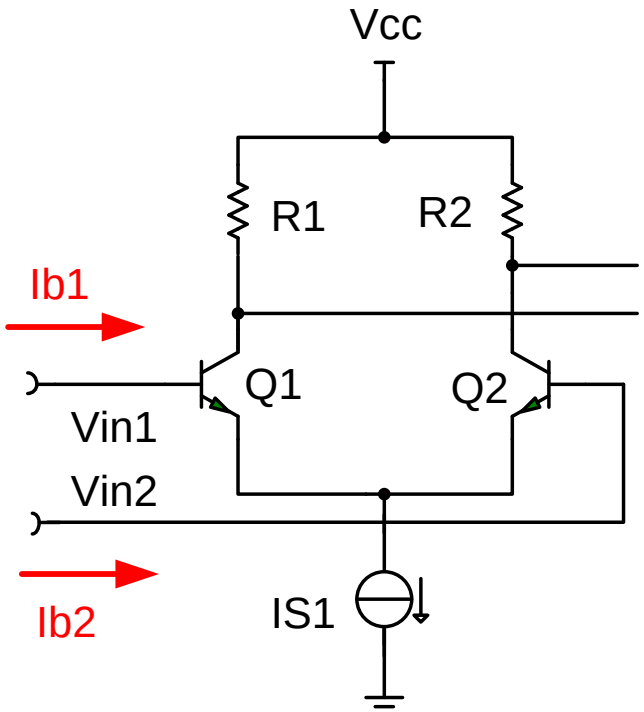
Input bias offset current:

$I_{B\_OS} = I_{B1} – I_{B2}$ = 210 nA – 150 nA = **60 nA**

Let’s now move on to input bias current, or I_B, and input bias current drift.

Input bias current is the current flowing into the inputs of an op amp. These currents can be modeled as a current source connected to each input, as shown in this figure. Ideally, the two input bias currents would be equal to each other and would cancel. In reality, though, they are not equal, and the difference of these currents is defined as input offset current. If the input offset current is low, it’s possible to match the impedances connected to each input and cancel the offset developed from the input bias currents.

Simple Bipolar, No I_B Cancellation

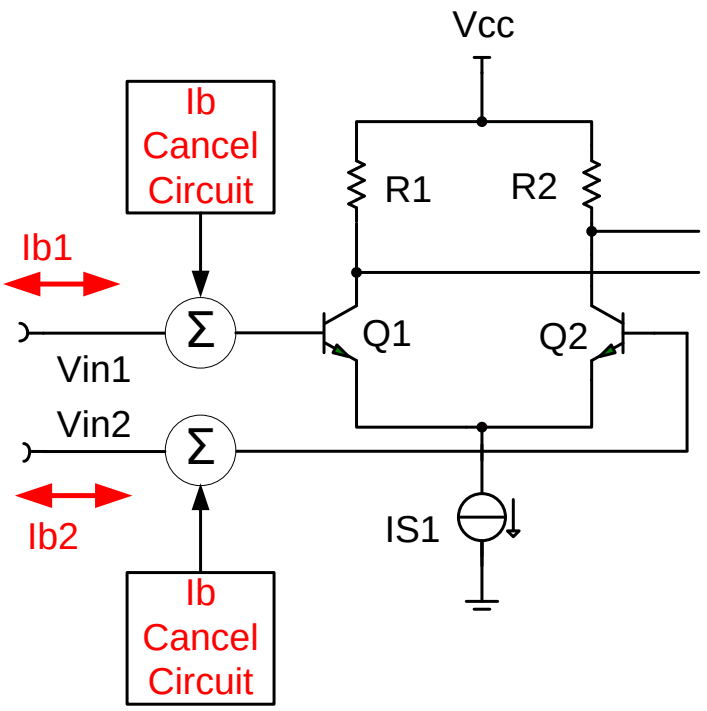


Bias current in bipolar amplifiers is from input transistor base current. It is typically larger than in FET-input amplifiers and it flows into the input terminals.

Parameter	Test Conditions	LM741C			Units
		Min	Typ	Max	
Input Offset Current	T_A = 25°C		20	200	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			300	nA
Average Input Offset Current Drift					nA/°C
Input Bias Current	T_A = 25°C		80	500	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			0.8	µA

In a bipolar amplifier, input bias current is the current flowing into the base of each transistor in the input pair. Generally, the bias current for bipolar amplifiers is larger than the bias current for MOSFET and JFET amplifiers. Typical numbers are in the nA range. You can see in the case of the LM741C, the input offset current is about 200nA max, and the input bias current is about 500nA max.

Bipolar with I_B Cancellation



The input bias currents are mirrored and summed back in to cancel the bias current. This has the effect of significantly reducing input I_B. Note that when this is done, I_B can flow in both directions. Also, I_{B_OS} is no longer smaller than I_B.

$$I_{B\_OS} = I_{B1} - I_{B2}$$

PARAMETER		CONDITION	OPA277P, U OPA2277P, U MIN	TYP(1)	MAX	
INPUT BIAS CURRENT						
Input Bias Current	I_B			±0.5	±1	nA
T_A = –40°C to +85°C					±2	nA
Input Offset Current	I_{OS}			±0.5	±1	nA
T_A = –40°C to +85°C					±2	nA

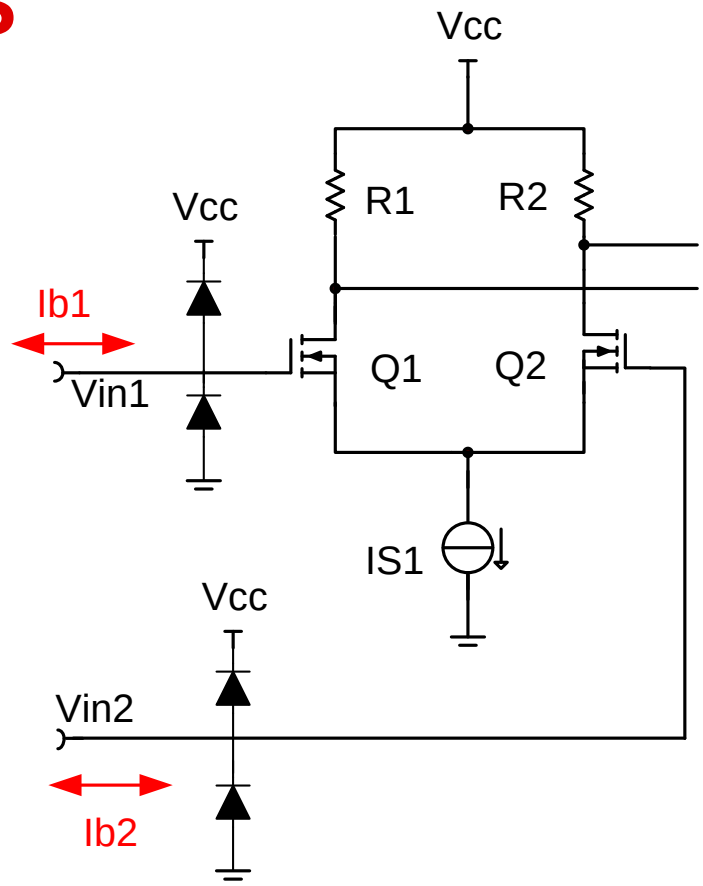
Some precision bipolar op amps use a method called bias current cancellation in order to minimize bias current. This is done inside the op amp, so no external components are required. The amplifier simply behaves like a bipolar amplifier with very low bias current.

Bias current cancellation is done by measuring the input bias current and summing in and equal, but opposite currents which cancel the bias current. This effectively takes an amplifier with hundreds of nA of bias current down to single nA of bias current.

You can see from the specification table in this example that the input bias current of the OPA277 is ±1nA maximum. In the previous example the bias current had to flow into the base of the transistor so the bias current could have only one polarity. In this case, however, the bias current can have either polarity, since the bias current cancelation circuit is not perfect and it's not known whether the polarity of the residual current will be positive or negative.

Bias Current for CMOS

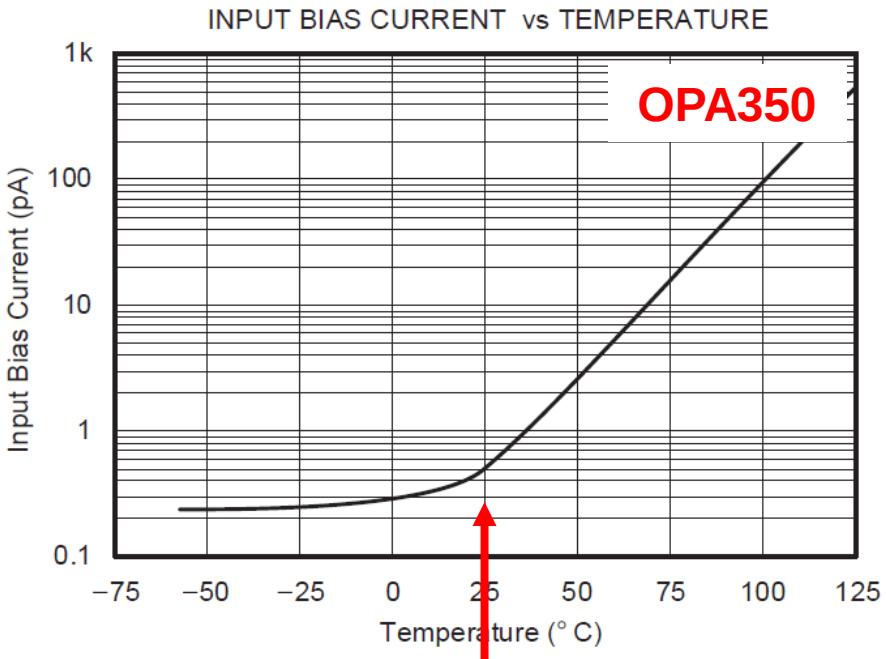
Bias current in FET-input amplifiers is mainly from leakage into ESD protection diodes.

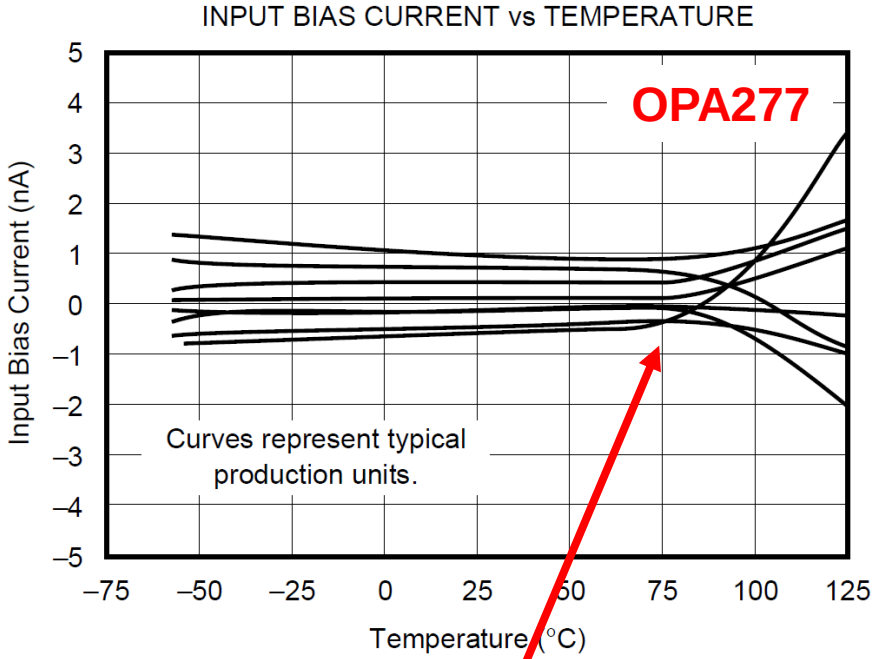


PARAMETER		CONDITIONS	OPA369, OPA2369			UNIT
			MIN	TYP	MAX	
INPUT BIAS CURRENT						
Input Bias Current	I_B			10	50	pA
over Temperature				See Figure 16		**pA**
Input Offset Current	I_{OS}			10	50	pA

In the case of MOSFET or JFET op amps, the input bias current is primarily due to the leakage of the input ESD protection diodes. The gate of the input MOSFET transistors has extremely low leakage, so it doesn't contribute significant bias current. You can see in this example that the OPA369 has 50pA max of input bias current.

I_B over Temperature





CMOS amplifier:

In this case you see a dramatic increase in bias current at 25 °C. Note the logarithmic graph, which doubles every 10 °C.

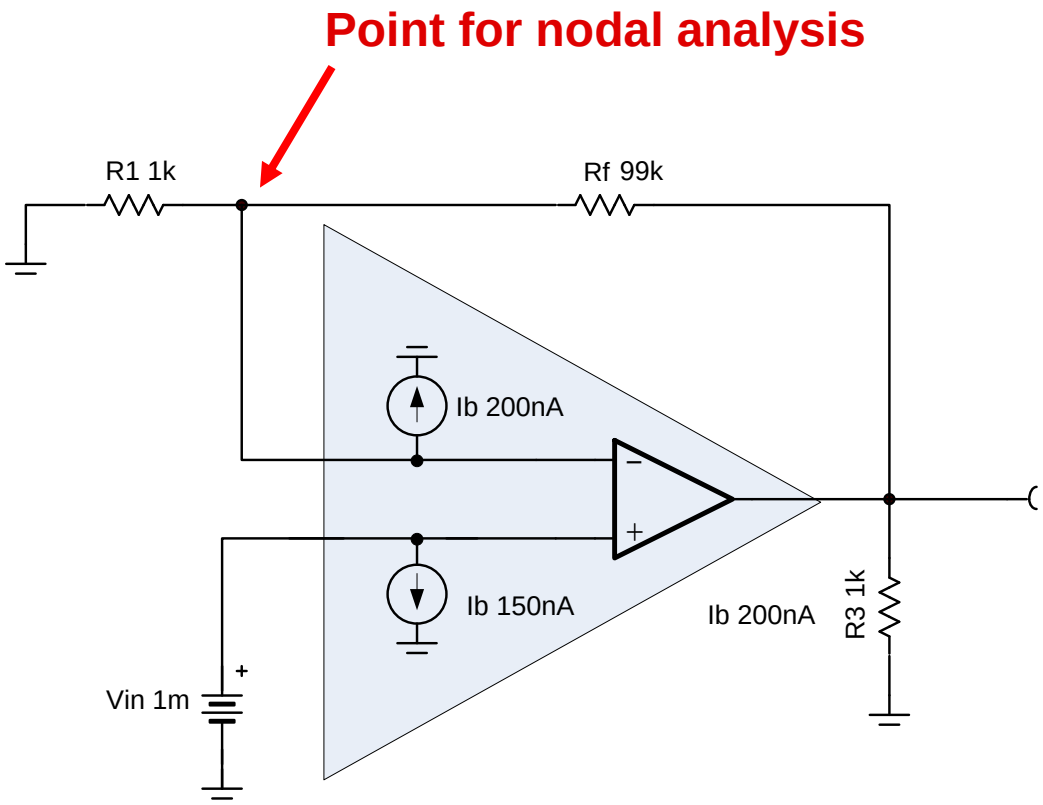
Bipolar amplifier:

In this case you see a dramatic increase in bias current at 75 °C.

One thing to remember with low bias current amplifiers is the effect of I_B over temperature. In MOSFET amplifiers, the bias current can double every 10°C. You can see in the example on the left with the OPA350 that the input bias current increases significantly at temperatures above 25°C. If you only considered the room temperature value of I_B and then operated the amplifier at elevated temperature, you would have significant errors. Notice that the vertical axis of the plot uses a logarithmic scale.

With the bipolar amplifier, the initial input bias current at room temperature is often large enough such that the relative change in input bias current over temperature is minimized. You can see in the example on the right with the OPA277 that the input bias current starts to increase at temperatures above 75°C, but note that the vertical axis uses a linear scale.

I_B Calculation – OPA211 at High Temp.



Using nodal analysis

$$\frac{V_{in}}{R_1} + \frac{V_{in} - V_{out}}{R_f} + I_b = 0$$

$$V_{out} = R_f \cdot \left(I_b + \frac{V_{in}}{R_1} + \frac{V_{in}}{R_f} \right)$$

Using superposition set Vin=0V

$$V_{out} = R_f \cdot \left(I_b + \frac{0}{R_1} + \frac{0}{R_f} \right) = I_b \cdot R_f$$

In this example

$$V_{out\_Ib} = (200nA) \cdot (99k\Omega) = 20mV$$

$$V_{out\_vin} = 1mV \cdot \left(\frac{99}{1} + 1 \right) = 100mV$$

$$V_{out\_total} = 20mV + 100mV = 120mV$$

This bias current calculation is very similar to what was done for offset voltage. First, we model the bias currents as two current sources connected to the op amp inputs. Note that the input bias current connected to the non-inverting input is flowing back into the input signal source, and since there is no source resistance, that bias current source doesn't add any error. If there were a source resistance connected to the non-inverting input, the bias current **would** generate an error voltage.

The error in this configuration arises entirely from the input bias current source on the **inverting** input which flows into the feedback network of R_1 and R_F. If we perform a nodal analysis, we can see that the output voltage caused by I_B is equal to I_B multiplied by R_F. We can then calculate the output caused by I_B and the output from the input signal. Using superposition, we can add the output signal from the bias current (equal to 20mV), and the output signal from the input source (100mV), since they are independent. In this example, the total output voltage equals 120mV and the error introduced by the input bias current is 20%.

Please keep in mind that this was an error calculation using high temperature I_B values. If this calculation was done at room temperature, the error would have been significantly smaller.

Range of Bias Current – fA to nA

Op Amp	I_B (max) (high grade)	I_B at max temp.	Technology
OPA129	100 fA	20 pA (typ.)	Difet – Ultra Low Bias Current
OPA627	5 pA	1nA	Difet – Precision High Speed
OPA350	10 pA	500 pA (typ.)	CMOS
OPA827	50 pA	50 nA max	JFET input, Bipolar, Precision
OPA333	70 pA	150 pA (typ)	Zero Drift CMOS
OPA277	1 nA	2 nA (max)	Precision Bipolar
OPA211	125 nA	200 nA	Precision Bipolar
OPA835	400 nA	530 nA	High Speed Bipolar
LM741	80 nA	0.2 µA (max)	Bipolar commodity (lower cost)

This table gives a range of input bias currents for different TI op amps.

Values can range from fA for specialized CMOS amplifiers, all the way up to hundreds of nA for high speed and commodity op amps.

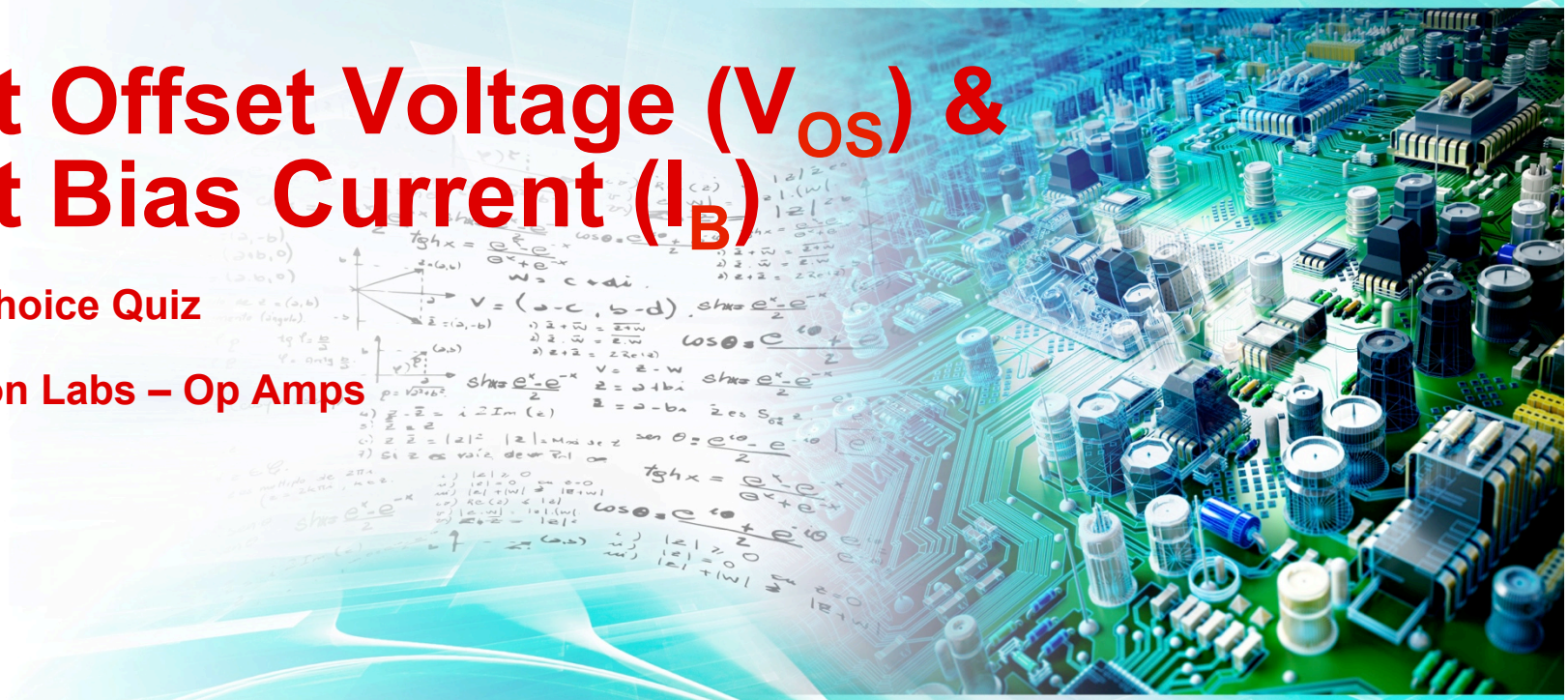
Note that bipolar op amps will always have higher input bias currents then CMOS amplifiers. Also, bipolar amplifiers with bias current cancellation circuitry, such as the OPA277, will have lower input bias current then bipolar op amps with out cancelation, such as the OPA211.

Thanks for your time!
Please try the quiz.

Input Offset Voltage (V_{OS}) & Input Bias Current (I_B)

Multiple Choice Quiz

TI Precision Labs – Op Amps



Texas Instruments

Quiz: Input Offset Voltage (V_{OS}) & Input Bias Current (I_B)

1. Which amplifier would have the highest bias current?

a. CMOS
b. Bipolar
c. Bipolar with input bias cancellation.
d. High speed.

2. Which amplifier would have the lowest offset voltage?

a. Zero drift amplifier
b. High speed CMOS
c. High speed bipolar

3. Texas Instruments SPICE models target the _____ specifications.

a. Maximum
b. Typical
c. High grade
d. Low grade

Quiz: Input Offset Voltage (V_{OS}) & Input Bias Current (I_B)

4. A typical offset of 10uV indicates _____.

a. The average offset is 10uV
b. 100% of the devices will have an offset less than 10uV
c. 50% of the devices will have an offset less than 10uV
d. standard deviation is equal to +/-10uV

5. A maximum offset of 100uV indicates _____.

a. 90% of the devices are less than 100uV.
b. The device was tested with 100uV limits and only passing units were c. shipped.
c. Applying more than 100uV will damage the unit.
d. Offset can range from 0 to 100uV

6. Bias current is modeled as _____

a. A current source in series with each input.
b. A current source connected to each input with respect to ground.
c. A resistance between the amplifier inputs.

Quiz: Input Offset Voltage (V_{OS}) & Input Bias Current (I_B)

7. Which are examples of an op amp test condition?

a. The maximum allowable input signal, and maximum supply.
b. The input common mode voltage, output load, and power supply voltage.
c. The input bias current, input offset current, and offset voltage.
d. Amplifier gain bandwidth and slew rate.

8. What is a factor that can affect bias current?

a. Supply voltage
b. Input signal voltage.
c. Temperature
d. Input offset voltage

9. Which is the primary cause of bias current in a CMOS amplifier?

a. ESD diode leakage.
b. Gate leakage
c. Parasitic capacitance
d. Semiconductor defects

Quiz: Input Offset Voltage (V_{OS}) & Input Bias Current (I_B)

10. Offset voltage can range from ____.

a. fV to nV
b. pV to uV
c. uV to mV
d. mV to V

11 Bias current can range from ___.

a. fA to nA
b. pA to mA
c. uA to A

12. Bias current cancellation is a technique ___.

a. Used in CMOS amplifiers to cancel Ibos.
b. Used in Bipolar amplifiers to minimize bias current.
c. An external circuit used to cancel op amp bias current.

Quiz: Input Offset Voltage (V_{OS}) & Input Bias Current (I_B)

13. What type of circuit would have the largest error from bias current.

a. A bipolar amplifier with a small source resistance.
b. A bipolar amplifier with a large source resistance.
c. A CMOS amplifier with a small source resistance.
d. A CMOS amplifier with a large source resistance.

14. Input offset voltage drift is _____.

a. A change in offset voltage over temperature
b. A change in offset voltage over time.
c. A change in offset voltage with different common mode voltages
d. A change in offset voltage with different power supply voltages.

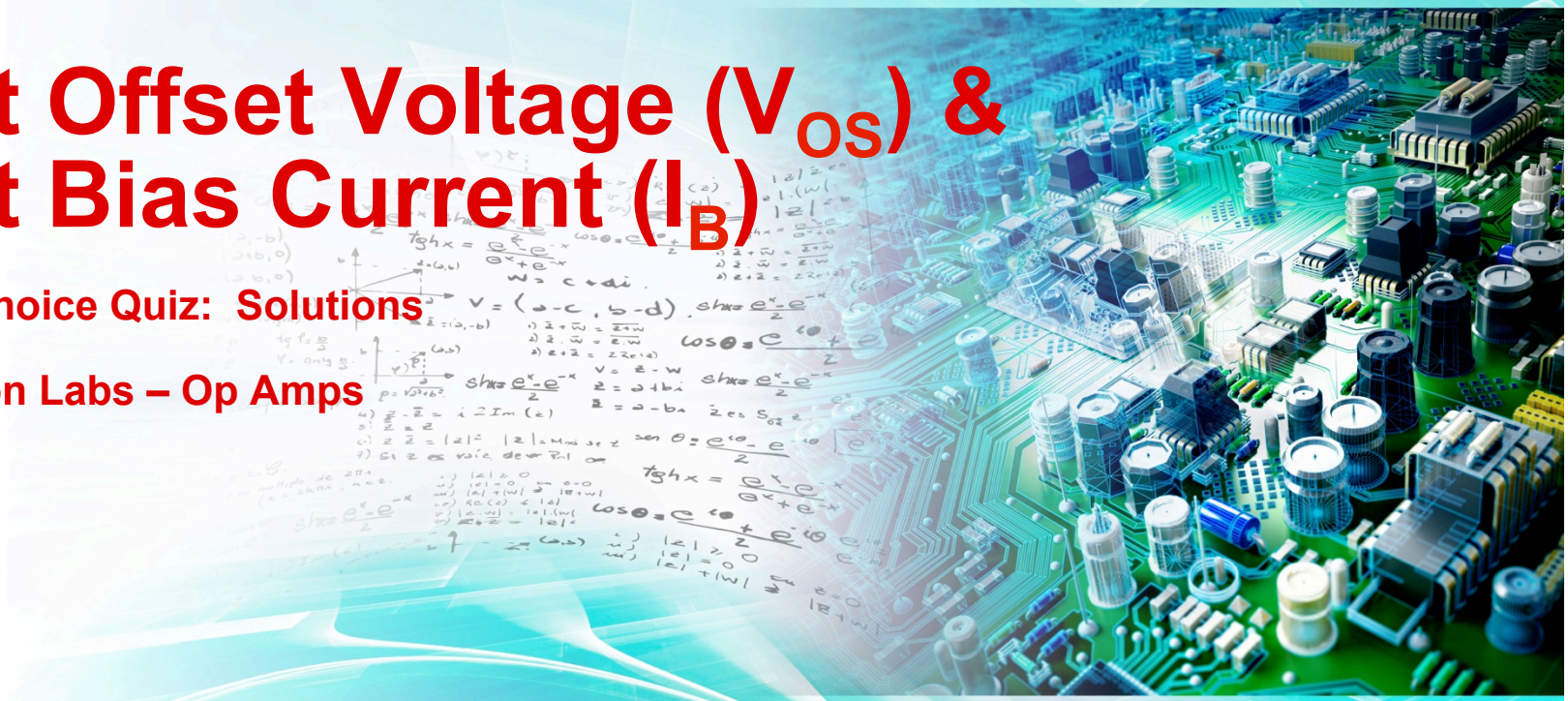
15 If a maximum specification is not given you can estimate the maximum by ____.

a. Multiplying the input by 10.
b. Doubling the typical
c. Looking at the distribution.
d. Comparison to similar devices.

Input Offset Voltage (V_{OS}) & Input Bias Current (I_B)

Multiple Choice Quiz: Solutions

TI Precision Labs – Op Amps



Texas Instruments

Input Offset Voltage (V_{OS}) & Input Bias Current (I_B) Quiz Solution

1. Which amplifier would have the highest bias current?

a. CMOS
b. Bipolar
c. Bipolar with input bias cancellation.
d. High speed.

2. Which amplifier would have the lowest offset voltage?

a. Zero drift amplifier
b. High speed CMOS
c. High speed bipolar

3. Texas Instruments SPICE models target the _____ specifications.

a. Maximum
b. Typical
c. High grade
d. Low grade

Input Offset Voltage (V_{OS}) & Input Bias Current (I_B) Quiz Solution

4. A typical offset of 10uV indicates _____.

a. The average offset is 10uV
b. 100% of the devices will have an offset less than 10uV
c. 50% of the devices will have an offset less than 10uV
d. standard deviation is equal to +/-10uV

5. A maximum offset of 100uV indicates _____.

a. 90% of the devices are less than 100uV.
b. The device was tested with 100uV limits and only passing units were shipped.
c. Applying more than 100uV will damage the unit.
d. Offset can range from 0 to 100uV

6. Bias current is modeled as _____

a. A current source in series with each input.
b. A current source connected to each input with respect to ground.
c. A resistance between the amplifier inputs.

Input Offset Voltage (V_{OS}) & Input Bias Current (I_B) Quiz Solution

7. Which are examples of an op amp test condition?

a. The maximum allowable input signal, and maximum supply.
b. The input common mode voltage, output load, and power supply voltage.
c. The input bias current, input offset current, and offset voltage.
d. Amplifier gain bandwidth and slew rate.

8. What is a factor that can affect bias current?

a. Supply voltage
b. Input signal voltage.
c. Temperature
d. Input offset voltage

9. Which is the primary cause of bias current in a CMOS amplifier?

a. ESD diode leakage.
b. Gate leakage
c. Parasitic capacitance
d. Semiconductor defects

Input Offset Voltage (V_{OS}) & Input Bias Current (I_B) Quiz Solution

10. Offset voltage can range from ____.

a. fV to nV
b. pV to uV
c. uV to mV
d. mV to V

11. Bias current can range from ___.

a. fA to nA
b. pA to mA
c. uA to A

12. Bias current cancellation is a technique ___.

a. Used in CMOS amplifiers to cancel Ibos.
b. Used in Bipolar amplifiers to minimize bias current.
c. An external circuit used to cancel op amp bias current.

Input Offset Voltage (V_{OS}) & Input Bias Current (I_B) Quiz Solution

13. What type of circuit would have the largest error from bias current.

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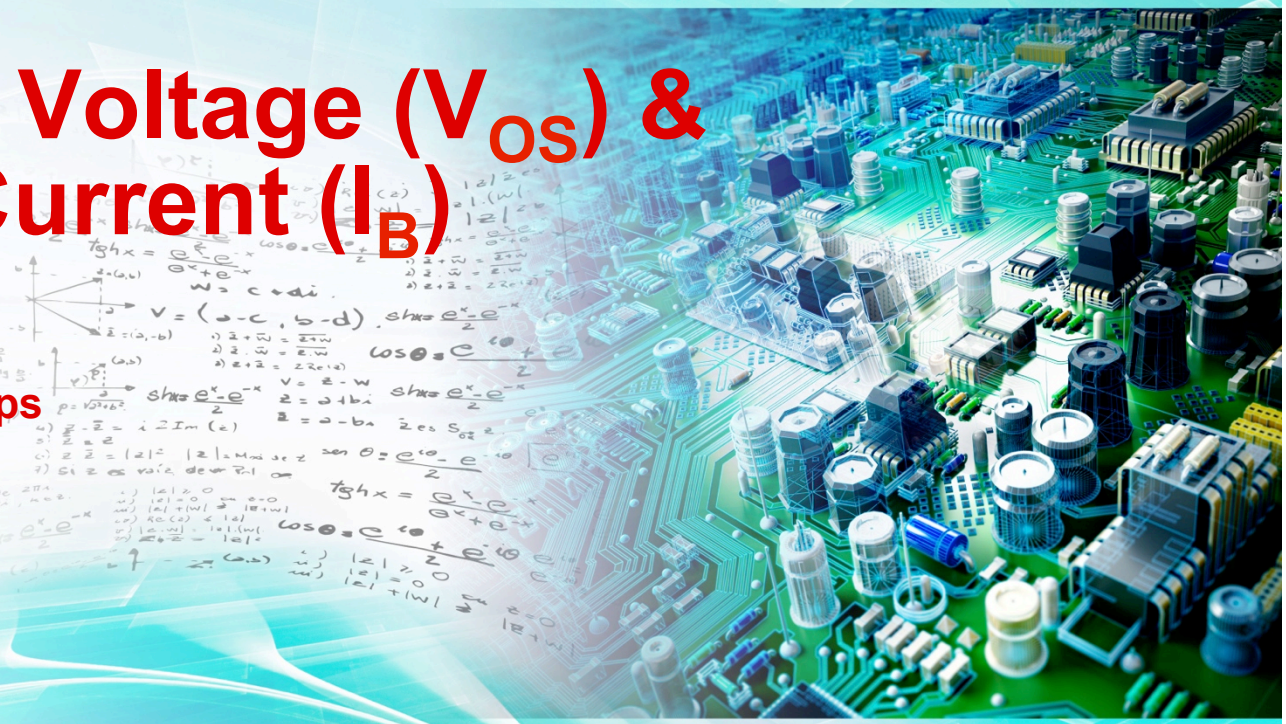
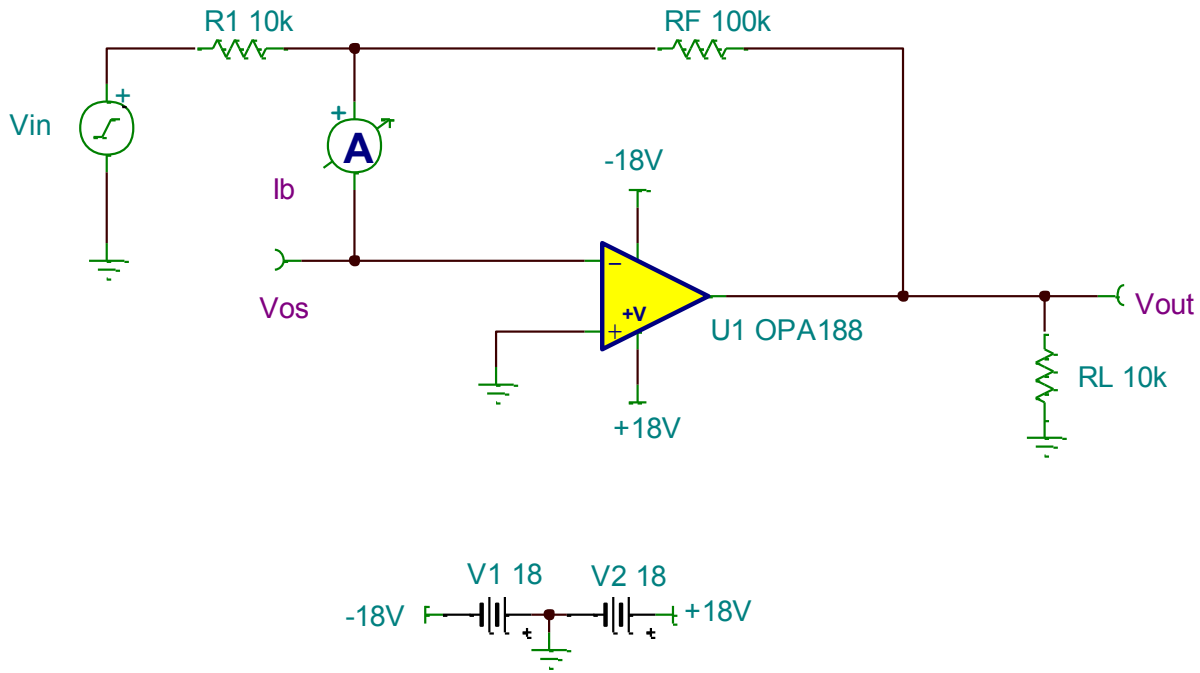
Input Offset Voltage (V_{OS}) & Input Bias Current (I_B)

Exercises

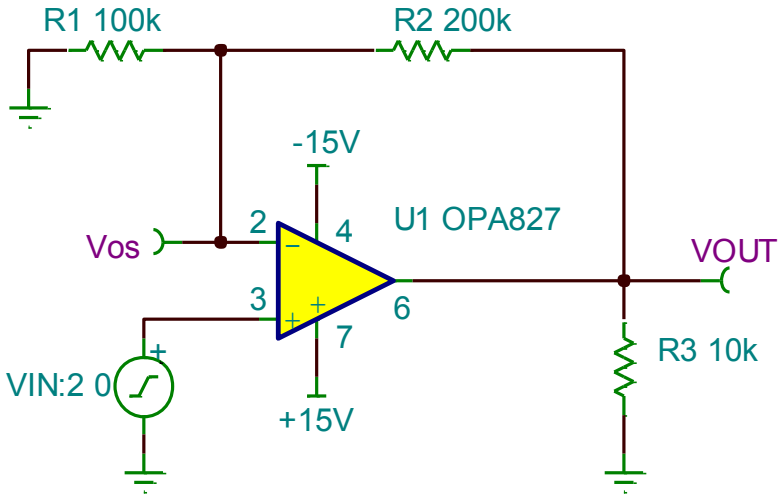
TI Precision Labs – Op Amps



1. Assume T = 25C. Find the output voltage from typical input offset voltage for the circuit below. Find the output voltage from input bias current. Add the two output to find the output from both effects (i.e. use superposition). Check your results with simulation. What is the dominant source of error.

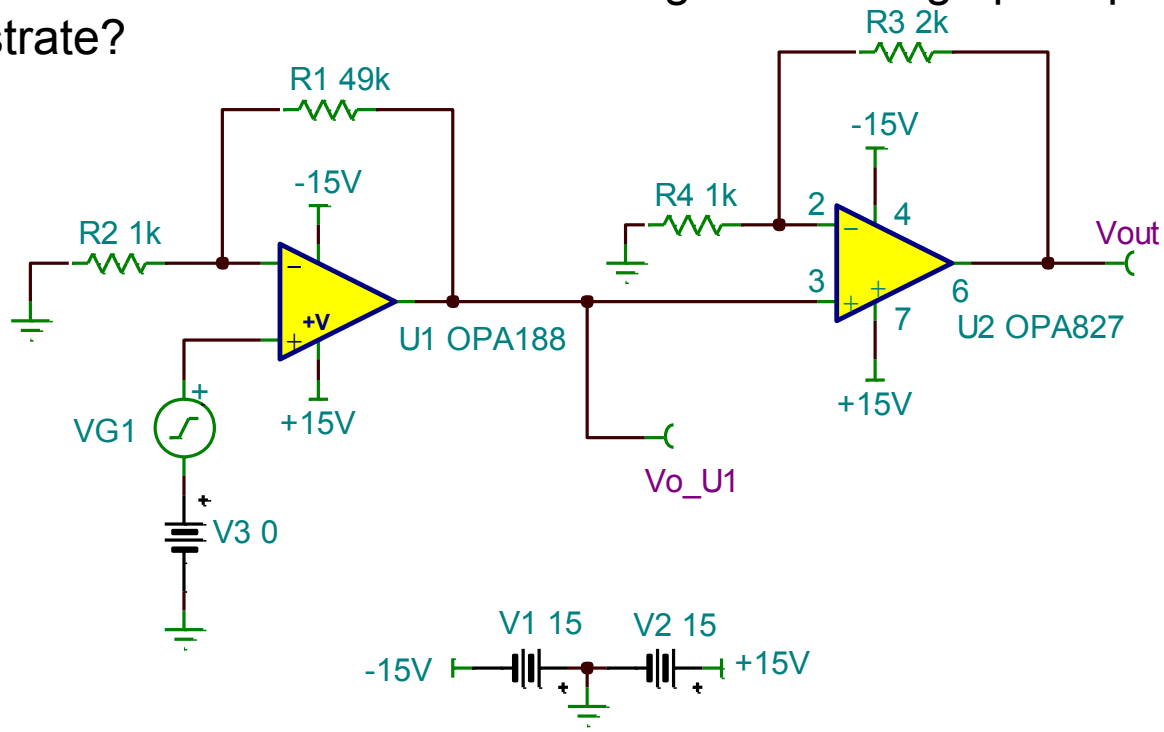


2. Calculate the output voltage for the circuit below from offset voltage and bias current (for T = 25C). Test with simulation. Calculate the output for T = 125C. Note the current simulation models don't account for temperature drift, so it is not possible to simulate at 125C. What is the dominant source of error at T = 125C?

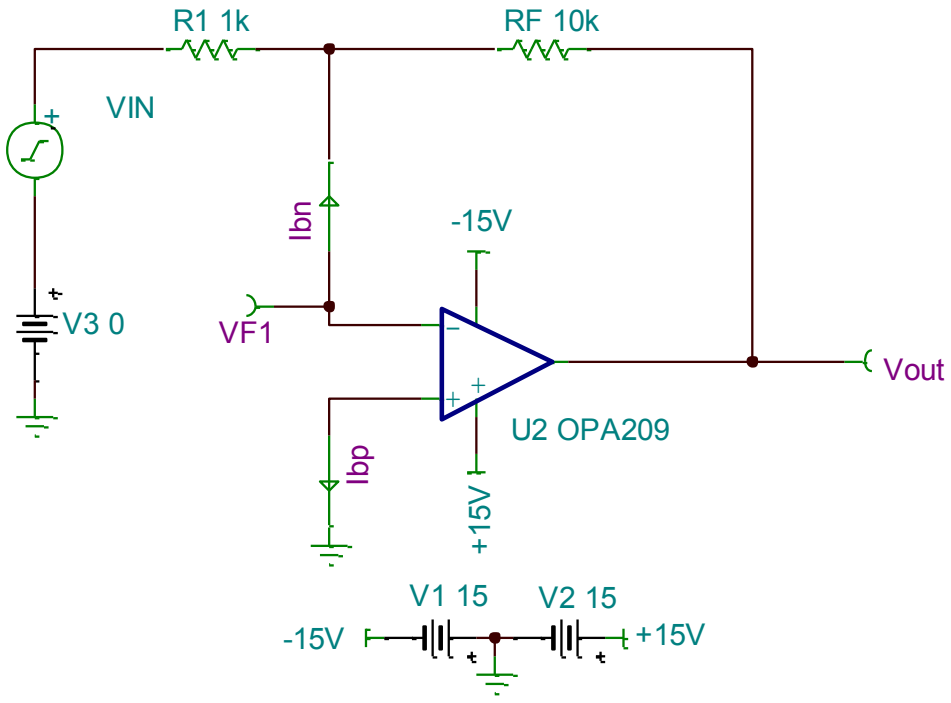


3. Calculate the output voltage for the circuit below from offset voltage and bias current (for T = 25C). Test with simulation. Switch the position of U1 and U2 (i.e. U1 = OPA827 and U2 = OPA188). Repeat the calculations and simulations.

Explain why the results are different? What general design principle does this example illustrate?



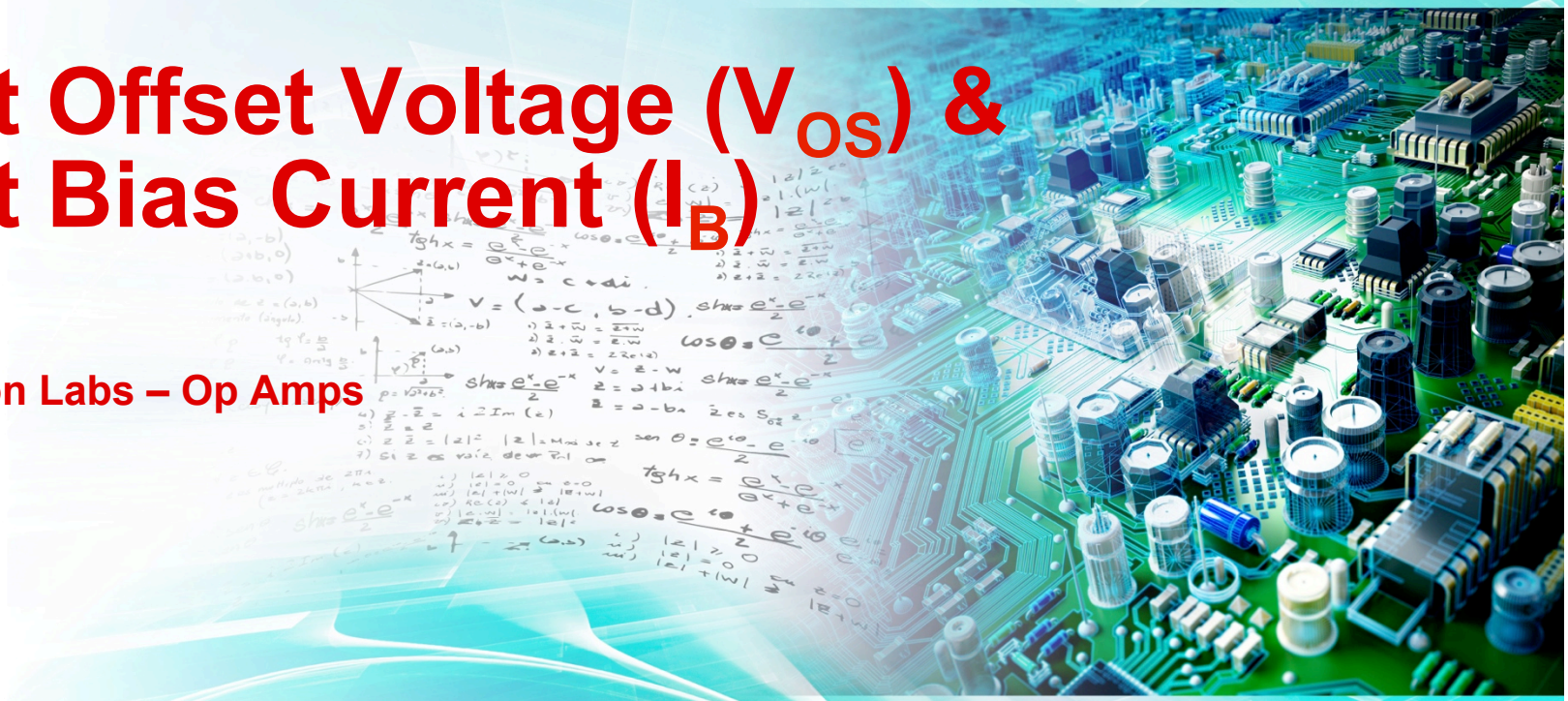
4. Solve the problem below for typical and maximum offset. Can this result be confirmed with simulation?



Input Offset Voltage (V_{OS}) & Input Bias Current (I_B)

Solutions

TI Precision Labs – Op Amps



Solution: Problem 1.

1. Below is the calculation for output due to Ib and Vos. Note that Ib and Vos can have any polarity so there are four possible answers. Also note that the typical values at 25C were used for the calculation. The dominant source of error is Vos; however, both Ib and Vos contributions are significant.

$$V_{out\_Ib} = I_b * R_f = (\pm 160pA) * (100k\Omega) = \pm 16\mu V \quad \text{Output from Ib}$$

$$V_{out\_vos} = \left[\frac{R_f}{R_1} + 1\right] * V_{os} = \left(\frac{100k\Omega}{10k\Omega} + 1\right) * (\pm 6\mu V) = \pm 66\mu V \quad \text{Output from Vos}$$

$$V_{out} = V_{out\_Ib} + V_{out\_vos} = \pm 16\mu V \pm 66\mu V \quad \text{Combined output}$$

$$V_{out} = V_{out\_Ib} + V_{out\_vos} = 16\mu V + 66\mu V = 82\mu V \quad \text{Case 1}$$

$$V_{out} = V_{out\_Ib} + V_{out\_vos} = 16\mu V - 66\mu V = -50\mu V \quad \text{Case 2}$$

$$V_{out} = V_{out\_Ib} + V_{out\_vos} = -16\mu V + 66\mu V = 50\mu V \quad \text{Case 3}$$

$$V_{out} = V_{out\_Ib} + V_{out\_vos} = -16\mu V - 66\mu V = -82\mu V \quad \text{Case 4}$$

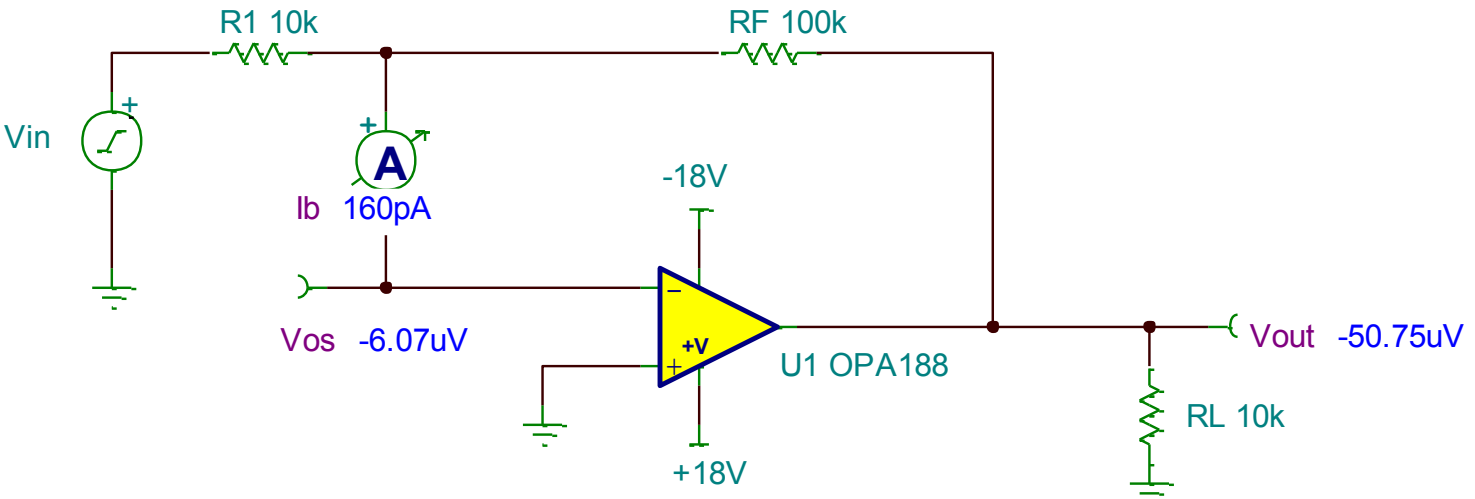
ELECTRICAL CHARACTERISTICS:
High-Voltage Operation, V_S = ±4 V to ±18 V (V_S = +8 V to +36 V)

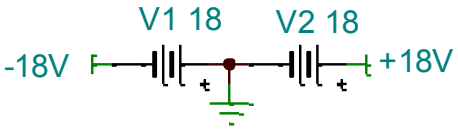
At T_A = +25°C, R_L = 10 kΩ connected to V_S / 2[1], and V_{CM} = V_{OUT} = V_S / 2[1], unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			±6	±25	µV
		T_A = –40°C to +125°C		±0.03	±0.085	µV/°C
PSRR	Power-supply rejection ratio	V_S = 4 V to 36 V, T_A = –40°C to +125°C		±0.075	±0.3	µV/V
	Long-term stability[2]			4		µV
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S / 2		±160	±1400	pA
		T_A = –40°C to +125°C			±8	nA

Solution: Problem 1 (continued)

1. Below are the simulation results for problem 1. The output voltage from bias current and the output from offset voltage appose each other as in Case 2 from the previous page. Note that the model could have been developed according to any of the cases on the previous page.





1100 - Vos and Ib - Problem 1.TSC

Solution: Problem 2

2. The solution for this problem is the same as problem 1. However, notice that Ib doesn't have a significant affect on this problem. This is because the OPA827 has JFET inputs (very low Ib).

$$V_{out\_Ib} = I_b * R_f = (\pm 3pA) * (200k\Omega) = \pm 0.6\mu V \quad \text{Output from Ib}$$

$$V_{out\_vos} = \left[\frac{R_f}{R_1} + 1\right] * V_{os} = \left(\frac{200k\Omega}{100k\Omega} + 1\right) * (\pm 75\mu V) = \pm 225\mu V \quad \text{Output from Vos}$$

$$V_{out} = V_{out\_Ib} + V_{out\_vos} = \pm 0.6\mu V \pm 825\mu V \quad \text{Combined output}$$

$$V_{out} = V_{out\_Ib} + V_{out\_vos} = 0.6\mu V + 225\mu V = 225.6\mu V \quad \text{Case 1}$$

$$V_{out} = V_{out\_Ib} + V_{out\_vos} = 0.6\mu V - 225\mu V = -224.4\mu V \quad \text{Case 2}$$

$$V_{out} = V_{out\_Ib} + V_{out\_vos} = -0.6\mu V + 225\mu V = 224.4\mu V \quad \text{Case 3}$$

$$V_{out} = V_{out\_Ib} + V_{out\_vos} = -0.6\mu V - 225\mu V = -225.6\mu V \quad \text{Case 4}$$

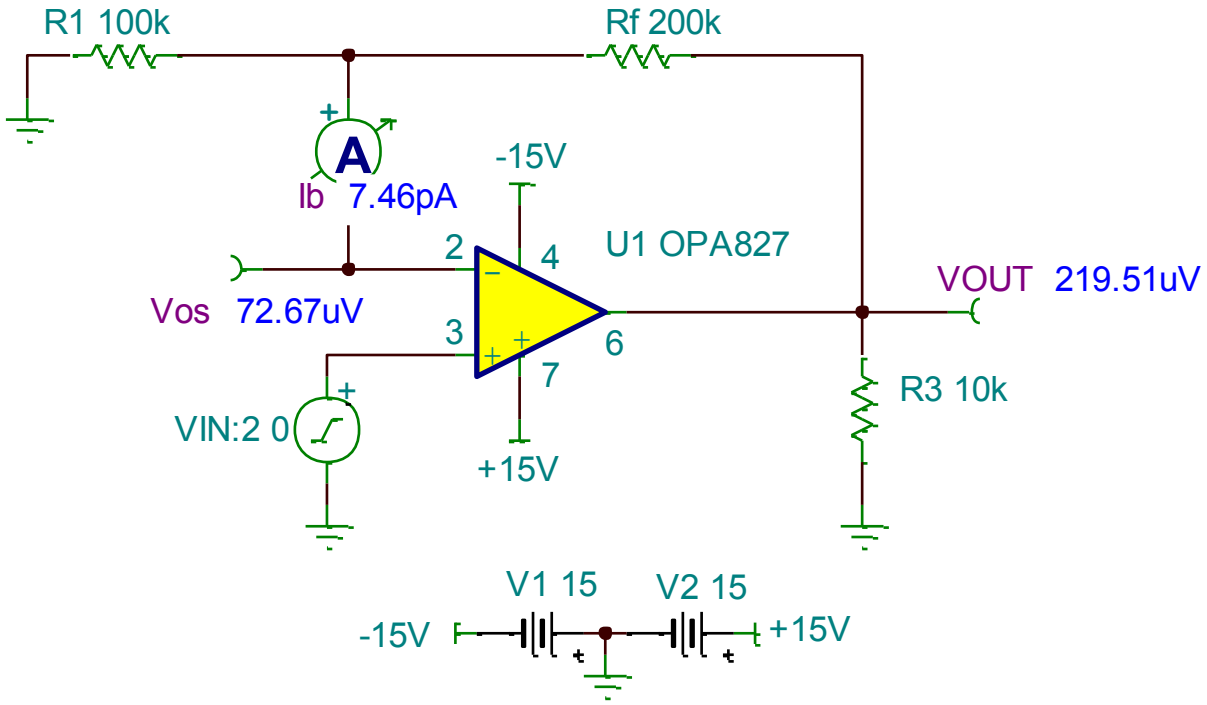
ELECTRICAL CHARACTERISTICS: V_S = ±4V to ±18V

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C**.
At T_A = +25°C, R_L = 10kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		CONDITIONS	OPA827AI MIN	OPA827AI TYP	OPA827AI MAX	UNIT
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = ±15V, V_{CM} = 0V		75	150	µV
Drift	**dV_{OS}/dT**			**0.1**	**2.0**	**µV/°C**
vs Power Supply	PSRR			0.2	1	µV/V
Over Temperature					**3**	**µV/V**
INPUT BIAS CURRENT						
Input Bias Current	I_B			±3	±10	pA
		–40°C to +85°C			±500	pA
Over Temperature		**–40°C to +125°C**			**±5**	**nA**

Solution: Problem 2 (continued)

2. Below is the simulation result for the circuit at room temperature. Notice that the values used for offset and bias current is close to the typical value but not exact. Model accuracy may be an issue in some cases so beware. However, in this case you can see that the output is relatively close to the expected result from the previous page.

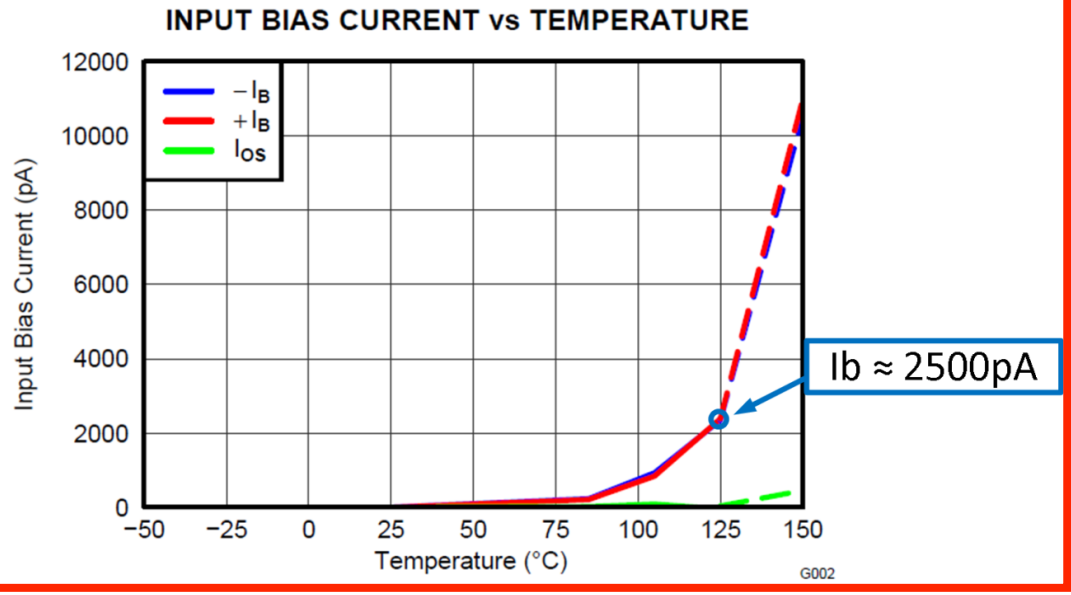


1100 - Vos and Ib – Problem 2.TSC

Solution: Problem 2 (continued)

2. In this section we calculate the offset voltage drift. The bias current drift is taken directly from the Ib vs temperature graph. Note that at high temperature bias current has become the dominant error source. This effect is often overlooked by engineers.

$\Delta V_{os\_T} = V_{os\_25C} + \Delta V_{os\_T} = \left(\pm 0.1 \frac{\mu V}{C}\right) * (125C - 25C) = \pm 10\mu V$	Change in offset
$V_{os\_125C} = V_{os\_25C} + \Delta V_{os\_T} = (\pm 75\mu V) + (\pm 10\mu V) = \pm 85\mu V \text{ or } \pm 65\mu V$	Offset at 125C
$V_{out\_vos} = \left[\frac{R_f}{R_1} + 1\right] * V_{os} = \left(\frac{200k\Omega}{100k\Omega} + 1\right) * (\pm 85\mu V) = \pm 255\mu V$	Output from offset at 125C
$V_{out\_Ib} = I_b * R_f = (\pm 2500pA) * (200k\Omega) = \pm 500\mu V$	Output from Ib at 125C
$V_{out} = V_{out\_Ib} + V_{out\_vos} = \pm 500\mu V \pm 255\mu V = \pm 755\mu V \text{ or } \pm 245\mu V$	Output from Ib and Vos at 125C



Solution: Problem 3.

3. Below is the hand solution and simulation result for the two stage amplifier. Note that there are eight different solutions because the polarity of bias current and offset voltage can be in either direction for either amplifier. The simulation result (-0.6mV) is close to one case in the hand calculation (-0.65mV). Also offset voltage is dominant.

$$V_{out\_vos} = \left\{\left[\frac{R_{f1}}{R_{i1}} + 1\right] * V_{os\_U1} + V_{os\_U2}\right\} * \left[\frac{R_{f2}}{R_{i2}} + 1\right]$$

Output due to Vos of each stage

$$V_{out\_vos} = \left\{\left[\frac{49k\Omega}{1k\Omega} + 1\right] * (\pm 6\mu V) + (\pm 75\mu V)\right\} * \left[\frac{2k\Omega}{1k\Omega} + 1\right]$$

$$V_{out\_vos} = 675\mu V \text{ or } 1.125mV$$

$$V_{out\_Ib} = \left[I_{b\_U1} * R_{f1}\right] * \left[\frac{R_{f2}}{R_{i2}} + 1\right] + I_{b\_U2} * R_{f2}$$

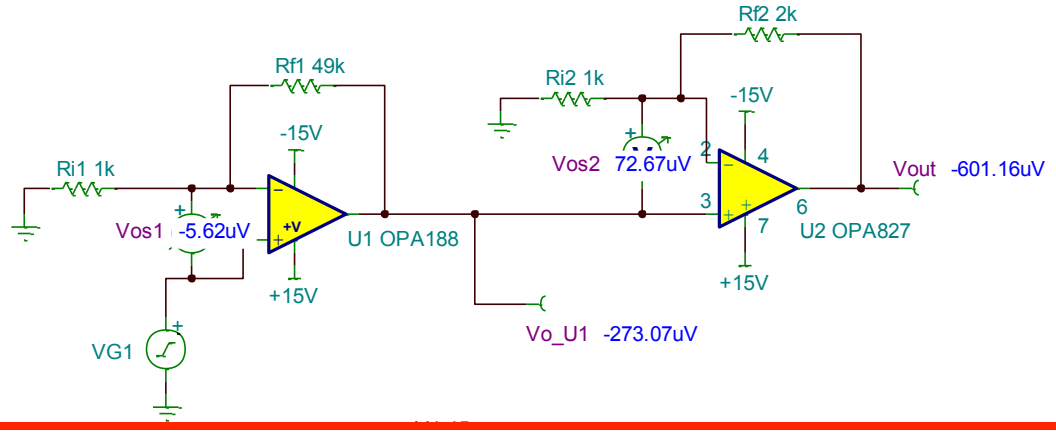
Output due to Ib of each stage

$$V_{out\_Ib} = \left[(\pm 160pA) * 49k\Omega\right] * \left[\frac{2k\Omega}{1k\Omega} + 1\right] + (\pm 3pA) * 2k\Omega$$

$$V_{out\_Ib} = \pm 23.5\mu V$$

$$V_{out} = V_{out\_vos} + V_{out\_Ib} = \pm 1.15mV \text{ or } \pm 1.10mV \text{ or } \pm 0.70mV \text{ or } \pm 0.65mV$$

Combined effect of Vos and Ib



1100 - Vos and Ib – Problem 3a.TSC

Solution: Problem 3 (continued)

3. Below the solution and simulation repeated with the OPA188 and OPA827 swapped. Note that the offset of the OPA827 is the dominant factor.

$$V_{out\_vos} = \left\{\left[\frac{R_{f1}}{R_{i1}} + 1\right] * V_{os\_U1} + V_{os\_U2}\right\} * \left[\frac{R_{f2}}{R_{i2}} + 1\right]$$

$$V_{out\_vos} = \left\{\left[\frac{49k\Omega}{1k\Omega} + 1\right] * (\pm 75\mu V) + (\pm 6\mu V)\right\} * \left[\frac{2k\Omega}{1k\Omega} + 1\right]$$

$$V_{out\_vos} = \pm 11.2mV$$

Output due to Vos of each stage

$$V_{out\_Ib} = \left[I_{b\_U1} * R_{f1}\right] * \left[\frac{R_{f2}}{R_{i2}} + 1\right] + I_{b\_U2} * R_{f2}$$

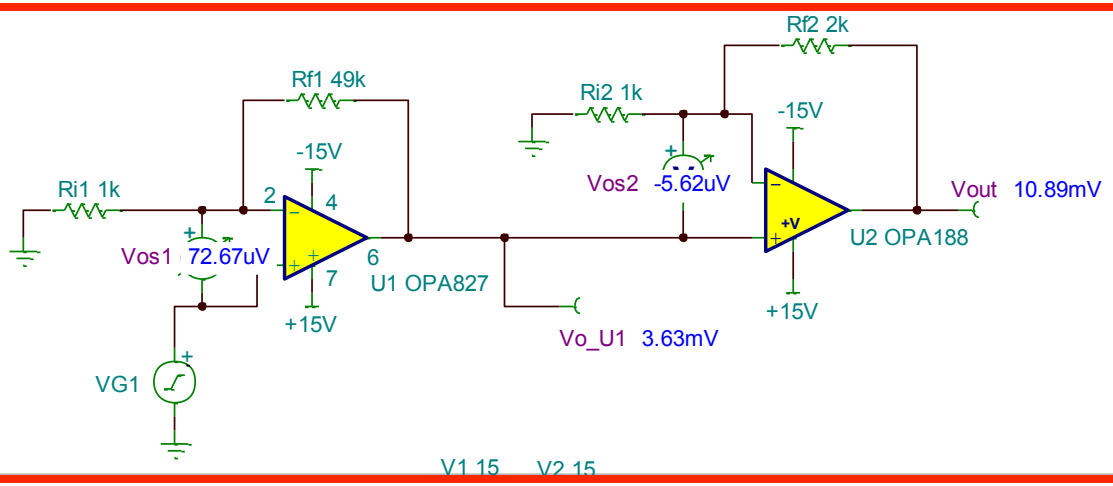
$$V_{out\_Ib} = \left[(\pm 3pA) * 49k\Omega\right] * \left[\frac{2k\Omega}{1k\Omega} + 1\right] + (\pm 160pA) * 2k\Omega$$

$$V_{out\_Ib} = \pm 0.76\mu V \text{ or } \pm 0.12\mu V$$

Output due to Ib of each stage

$$V_{out} = V_{out\_vos} + V_{out\_Ib} = \pm 11.2mV$$

Combined effect of Vos and Ib



1100 - Vos and Ib – Problem 3b.TSC

Solution: Problem 3 (continued).

3. In both cases Vos was the dominant factor. The offset from the first stage is amplified by both stages. In this case the first stage offset sees a total gain of 75 x 3. The second stage, on the other hand, only sees the second stage gain (3). Thus, the offset of the first sage dominates. This is why the output offset is substantially larger when the OPA827 is used in the first stage.

General Rule: It is best to use the lowest offset amplifier in the first stage to minimize offset.

Vout U1= OPA188, U2 = OPA827	Vout U1 = OPA827, U2 = OPA188
±1.15mV or ±1.10mV or ±0.70mV or ±0.65mV	±11.2mV

Amplifier	Vos	Ib
OPA188	6µV	160pA
OPA627	75µV	3pA

Solution: Problem 4.

3. Below the typical and maximum calculated output due to Ib and Vos. The simulation result shows typical.

Typical output due to Ib and Vos

$$V_{out\_Ib} = I_b * R_f = (\pm 1nA) * (10k\Omega) = \pm 10\mu V$$ Output from Ib typical

$$V_{out\_vos} = \left[\frac{R_f}{R_1} + 1\right] * V_{os} = \left(\frac{10k\Omega}{1k\Omega} + 1\right) * (\pm 35\mu V) = \pm 385\mu V$$ Output from Vos typical

$$V_{out} = V_{out\_Ib} + V_{out\_vos} = \pm 10\mu V \pm 385\mu V$$ Combined output typical

$$V_{out} = \pm 395\mu V \text{ or } \pm 375\mu V$$

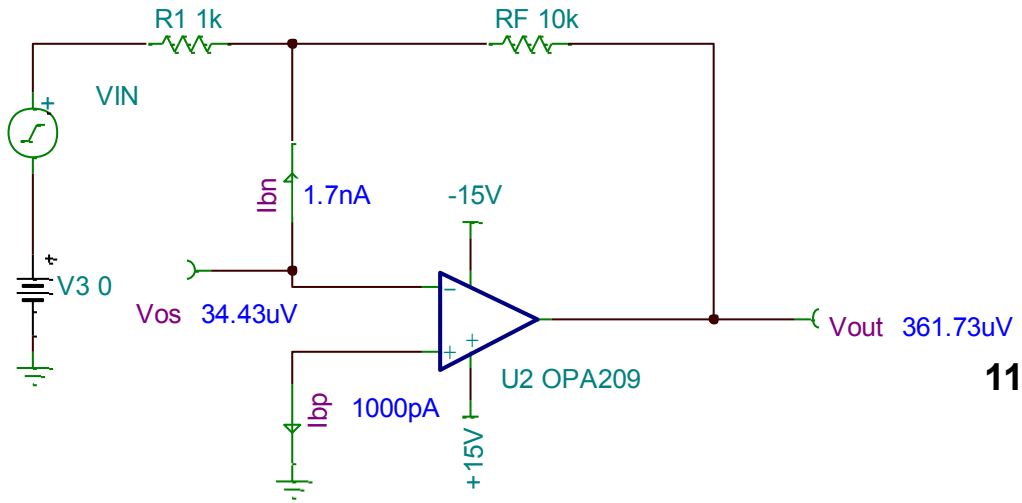
Maximum output due to Ib and Vos

$$V_{out\_Ib} = I_b * R_f = (\pm 4.5nA) * (10k\Omega) = \pm 45\mu V$$ Output from Ib Maximum

$$V_{out\_vos} = \left[\frac{R_f}{R_1} + 1\right] * V_{os} = \left(\frac{10k\Omega}{1k\Omega} + 1\right) * (\pm 150\mu V) = \pm 1650\mu V$$ Output from Vos Maximum

$$V_{out} = V_{out\_Ib} + V_{out\_vos} = \pm 45\mu V \pm 1650\mu V$$ Combined output Maximum

$$V_{out} = \pm 1.696mV \text{ or } \pm 1.605mV$$



1100 - Vos and Ib – Problem 4.TSC